The Chip Insider

July 10, 2001: From the front lines . . .

Road Test: Agilent's 93000 SOC tester series - - or 93K as many call it - - was thought by many to be just an extension of the company's existing product line. To some extent this is true, the 93K did rely on a platform that has proven to be very successful. The difference is that the 93K broke new ground in its heavy hitting combination of value, breadth, scalability, and performance. It's the big iron tester that broke the $1K per pin barrier; that can test everything from analog to logic and memory; that can be bought as a moderate cost 200MHz tester and then be scaled up to a full blown 1250 MHz screamer - - all with the same platform and software; and then achieve what is arguably the best jitter specs in the industry.

The 93K is Agilent's latest generation of a platform that has almost 1300 systems installed worldwide. Its older siblings, the 83000 and 94000, have been very successful, with roughly 1000 systems installed. The 93000 was first introduced as single tester targeted at SOC devices in July of 1999. However, it quickly became apparent that while SOC devices demanded the most of a tester, as the SOC chip market had an extreme range in performance and price. The classic big iron tester had the performance, but was too expensive to be cost effective across this range.

Any high-speed tester can test at low speed. But it costs a lot to build a high performance tester. The real challenge is to find a single platform than can hit low performance ranges at low cost and then have the legs to can extend your test floor out to high performance, albeit at high cost. One expects to pay a lot for high performance, but most would leave the Ferrari in the garage for Sunday drives and take the Lexus to work. Invariably you need two platforms. Typically one has to change platforms when more tester performance is needed and often the two platforms are not compatible. The test engineer faces all the problems of different systems and different software. Things like a simple design shrink can be a big headache it the new chip's performance is greater than the tester its original program was written on.

Agilent responded to this challenge last October when they unveiled the 93K as a series that offered unprecedented breadth of performance and price.

Agilent's 93000 SOC Tester Series

	Speed	Edge Placement Accuracy*	Price Per Pin**	Upgrades from Slower Model by . . .
	(Mbps)	(Ps)	($K)	
C200e	200	175	1 - 2	
C400e	400	175	2 - 3	Changing Software
P600	666	100	3 - 4	Changing Hardware
P800	800	100	5 - 6	Changing Software
P1000	1250	100	6 - 7	Changing Software
NPxxxx	- -			
NP2500	| *Look for it at SEMICON West* |			
NPxxxx	- -			

* All edges, formats, pins, periods, and data patterns
** For the typical range of pin configurations

Agilent achieves this range with a combination of hardware and software across two classes (C and P). The platform is the same, while the big differences are in the pin electronics and software. Speed upgrades within a class can be made with only a software change. Upgrading to a new class requires

changing the pin electronics, which also yields an accuracy gain. The cards in the C class testers use lower cost technology, which also explains why they are less accurate. It's not too tough to figure out that Moore's Law will drive future performance gains that will lead to new classes, call it new P or NP for lack of a better term. This brings up another key point. Agilent's architecture is highly dependent on semiconductor technology and its specialty chips come for Agilent's own fab. It is only tester manufacturer that has this capability and they use it to full advantage.

The advantage of the 93K's single platform is lower up-front costs, lower programming costs, and lower training costs. People only have to learn one system architecture. Test programs are fully transportable across the series. So, not only can it offer the wide range of requirements needed to test an SOC device, it can also test a wide range of components. If you talk to a 93K customer, invariably they will rate this capability high and will likely mention it first when asked what they like best about the tester - - though they often didn't buy it for this reason. It's just one of those pleasant surprises often realized only after buying a product.

But there are also performance advantages that accrue from the architecture. With their own chip making capability, Agilent takes Tester-Per-Pin concepts to an extreme level. Like everybody else, Agilent puts the DC parametrics, timing generators, error capture, PMU, and vector memory on each pin's electronics. Agilent prefers to put the AC-to-DC power conversion back in the support rack to avoid noise in the test head. The real difference is that Agilent also adds pattern generation and control as well as test sequencing capability to each digital pin. Most testers use a central sequencer that resides back in the mainframe. There is nothing new here. Agilent has been doing this since 1991. But as performance requirements rise, it becomes more important. For example, the patterns coming out of each pin of the test head can be dynamically adjusted to eliminate jitter. This jitter arises as each pin's signal diverges slightly in time as the pattern is sent across many pins and the electrical paths to the device vary. So, when the edges of every pin's signals are overlayed, an eye appears instead of nice clean square edges. As speed is upped, poor jitter performance will cause this eye to close, meaning that the pins are out of phase with each other. The signals arrive at different times inside the chip making garbage out of the test results.*** Having test sequencing per pin also means that BIST controllers can be driven independently in parallel. In fact, the chip can be broken up into its memory, logic, and analog sub-blocks and each can be exercised independently in parallel - - making for much faster test times.

So what do customers like about Agilent's 93000? "It's the best of the new generation machines for its system performance to cost ratio . . . it is a very cost effective machine." "I can go from 200Mhz to 1Ghz without switching platforms . . . this means long life. Switching platforms is very painful." "Good jitter performance for low cost." The 93K's strengths are its "range of capability, high frequency capability, accuracy, and stability." "The 93K's flexibility is its main strength. I can use the same platform to test high end and low end devices and still be cost effective." What do they say could be improved? Resoundingly they say it's the software. As one customer caustically put it, "They used to go by the slogan 'Just Enough Test.' Well we got just enough software to make it usable." Though others were more charitable, pointing out that "the series was still young and we knew the software would weak when we bought it." They point out that Agilent has been very responsive on this point and are working hard to improve it. "We went ahead and bought it because the other features were so overriding."

The bottom line is that the 93K offers great hardware, a wide range of capability, and it is extremely cost effective. These strengths well out weigh its weakness in software. If a silver bullet tester could be built, this could be it.

*** This is a is very important issue for SOC chips that use source synchronous buses, Network processors and SerDes (Serial/Deserializers).

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