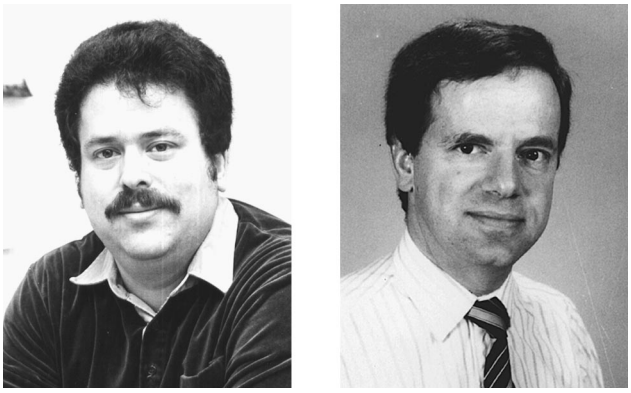

Figure 30. (*left*) Bernard Meyerson and (*right*) George Celler.

extensive monograph summarizing a number of cleaning technology and surface preparation processes and their relation to enhanced device performance.[368] The preparation of the silicon surface, cleaning, passivation, and surface morphology, has played a significant role in ensuring the development of improved device performance and yield.

Both polished and epitaxial wafers exhibit specific defects that must be controlled. Polished wafer defects include metal and organic surface chemical residues, particles, and grown-in microdefects, such as COPs. Epitaxial wafer defects include large structural defects ($>1\ \mu m$), (such as epitaxial stacking faults[192]) and small structural defects ($\leqslant 1\ \mu m$) as well as particles and residual chemical residues. Starting material requirements are expressed in terms of specific types of surface defects for different wafer types. The influence of the preoxidation clean on the SiO_2 growth rate, surface organics (apparently the carbon atom surface density) and its degrading effects on MOS GOI as well as the increased roughening of the silicon surface heated in a hydrogen ambient, compared to nearby surface regions covered with residual SiO_2 films, remain important arenas of research.[1] Indeed, the removal and prevention of surface defects is a current state-of-the-art challenge for silicon wafer technology with immense CoO implications. The development of laser scanning and other instrumentation to count, size, and determine the composition and morphology of these defects is a critical metrology challenge[369] and continues to be addressed by a variety of equipment and fab personnel.

IC Scaling

Gordon Moore's assessment of memory component growth in 1965, initially based on bipolar and then MOS memory density, was observed to quadruple every 2 years[20] (modified to ~3 years around the mid-later 1970s and currently taken as 3-4 years based on a 1995 assessment[21]), became enshrined as Moore's law. Indeed, Moore's law became the productivity criterion by which the IC industry grew at a 25% compound annual growth rate (CAGR). Device scaling has been the engine driving this revolution, with major contributions arising due to reductions in gate dielectric thickness, physical gate length and extension junction depth, as discussed by Robert Dennard and colleagues via constant electric-field scaling and, subsequently, constant voltage scaling.[370,371] These parameters were empirically related in 1980 by Simon Sze and colleagues;[372] Sze is the author of the influential textbook *Physics of Semiconductor Devices*.[373] For example, consider the scaling of the KDRAM from the early 1970s (4K DRAM) to today's leadership MPU part appropriate for the 100 nm technology generation in 2003.[22] The SiO_2 gate dielectric has proceeded from the range of 50-100 nm for the 4K DRAM to an anticipated value of about 1.2 nm oxide equivalent thickness (EOT) for the MPU part.[22] Likewise, the physical gate length has decreased from 7.5 μm for the 4K DRAM to a physical gate length of about 45 nm for the MPU part at the 100 nm technology generation.[22] Finally, the junction depth has decreased from several micrometers for the 4K DRAM to about 20 nm for the extension junction depth for the MPU part at the 100 nm technology generation.[22] In a related fashion, the critical figure of merit for transistor speed, CV/I, has become less than one psec for an NMOSFET and approaching one psec for a PMOSFET, as the physical gate length has decreased from 30 to 20 to 15 nm in leading edge research devices.[374]

Robert Dennard introduced the one-transistor memory cell in 1968,[375] thereby establishing the paradigm by which enhanced scaling has progressed. Scaling of the gate dielectric SiO_2 to the sub-2 nm regime, however, has exacerbated the occurrence of direct tunneling[376,377] as described by Yuan Taur and colleagues. An extensive global effort is in progress to identify an alternative, high-dielectric constant material to circumvent the gate dielectric direct tunneling leakage current in the case where the silicon oxynitride gate dielectric is less about 1.2 nm,[22,378-382] including the relevant diagnostic techniques as described by Diebold and colleagues.[19,383,384] Rajendra Singh, 1998 DS&T Callinan Awardee and co-editor of the ECS *Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues* proceedings and the Materials Research Society's (MRS) March, 2002 issue of the MRS Bulletin, as well as other Symposia, continues the focus on alternative, high-k gate dielectric matierlas, gate electrodes (eventually requiring dual metal gates with differing work functions for CMOS optimization) and the issues of incorporating the gate stack into an integrated, conventional planar, initially poly electrode, IC process flow. Additionally, Al Tasch (Fig. 29), Electronics Division Awardee in 1997, has clarified the role of the quantum confinement effect in silicon in increasing the effective dielectric thickness of a MOSFET in inversion,[385] which cannot be avoided as compared to the poly-depletion effect in the polysilicon gate electrode, which can be negated by utilizing metal gate electrodes. In that regard, a dual metal system with differing work functions is under consideration as the gate electrodes for optimal CMOS performance.[22]

Concurrently, a host of studies are in progress to identify an ultrashallow junction fabrication methodology consonant with the sub-100 nm technology generations.[22,386] These studies may be grouped under the classification as classical CMOS structures. On the other hand, a plethora of nonclassical CMOS devices are under consideration wherein a unique combination of materials and/or structural configuration of the device may differ from the conventional or classical planar CMOS structure.[22] Of particular importance is the assessment of alternate channels for enhancement of the n- and p-channel mobility, ranging from strained silicon on unstrained Si-Ge on SOI, silicon-germanium on silicon and a host of alternative vertical transistor structural configurations[387,388] as well as the ballistic transistor.[389]

Silicon-Germanium

The limitations of silicon electronic devices have warranted the development of compound semiconductors such as gallium arsenide with a larger electron and hole mobility as compared to silicon for specialized, mainly high frequency, electronic applications. The limited device integration possible with compound semiconductors, however, and the complexity of processing compound semiconductors has driven the extension of silicon technology by forming alloys of silicon with germanium as exemplified by Bernard Meyerson (Fig. 30), Electronics Division 1993 Awardee[390-392] and John Bean,[393] and their colleagues as well as other research groups. The silicon energy gap ($E_g = 1.12$ eV) at the X symmetry point can be monotonically decreased with the addition of germanium break ($E_g = 0.66$ eV). The flexibility of tuning the energy gap in silicon-germanium alloys can improve the performance of specialized, high performance electronic devices.[103]

In some cases, the germanium content is changed abruptly at a certain distance from the surface of the semiconductor to form an abrupt heterojunction, with a discontinuity in the energy gap. Because silicon and germanium have similar electron affinities, the

Figure 31. (*left*) Sorin Cristoloveanu and (*right*) Jim Meindl.

Figure 32. (*left*) Don Shaw and (*right*) Jerry Woodall.

energy required to remove an electron from the bottom of the conduction band to outside the crystal, of 4.05 and 4.00 eV, respectively, the conduction-band edge is nearly continuous at the silicon-germanium boundary, while the valence band edge has a discontinuity large enough to modify device performance. This valence-band discontinuity is especially useful in bipolar transistors. The gain of an npn bipolar transistor is related to the ratio of the electron current injected across the emitter-base junction to the sum of the electron and hole currents crossing that junction. The valence-band discontinuity creates a barrier which decreases the injection of holes from the base into the emitter, thereby increasing the gain of the transistor. A further approach to improving bipolar transistor performance is accomplished by increasing the germanium content gradually with position in the base layer. In this case, the energy gap varies as a function of position across the base region of the transistor. The varying energy gap creates an internal electric field which accelerates the free carriers (*i.e.*, electrons in the case of an npn transistor) across the base region, thereby increasing the maximum frequency response, f_t, of the bipolar transistor towards 100 Ghz.

A p-channel silicon MOS transistor has a small hole mobility. The hole mobility in silicon-germanium alloys, however, can be greater than in pure silicon.[393] The increased carrier mobility enhances the transconductance of the p-channel MOS transistor. Furthermore, in silicon-germanium p-channel MOS transistors a thin layer of silicon-germanium, slightly separated from the oxide-semiconductor interface by a silicon layer, can spatially confine holes. These confined holes travel in the silicon-germanium layer and, accordingly, their velocity is not reduced by scattering from the oxide-semiconductor interface.

Optimal electrical properties were achieved by ensuring the crystal bonding is uninterrupted across the silicon/silicon-germanium interface. The lattice constant of germanium, however, is ~4% greater than that of silicon. The lattice mismatch increases with increasing germanium content in silicon-germanium alloys. Modern growth techniques using CVD can form a thin layer of silicon-germanium alloy on silicon with a continuous crystal structure across the interface (*i.e.*, the crystal structure is commensurate). The alloy layer, however, is compressed in the plane of the film. With increasing layer thickness, the energy associated with compressing the alloy layer to fit the silicon crystal increases. Above a critical thickness,[394] the strain energy exceeds the energy necessary to form misfit dislocations. As the bonds across the interface break to form the misfit dislocations, the strain in the system is reduced, thereby lowering the total energy. Accordingly, although silicon-germanium layers thicker than the equilibrium critical thickness can be formed, they are unstable.[394] When these metastable layers are heated above the stability temperature appropriate to the layer thickness and germanium content, any irregularity already present can nucleate a misfit dislocation, taking into account kinetic considerations. The dislocation then propagates along the interface, creating a line of broken bonds. While misfit dislocations at the interface may be detrimental to device performance, interactions between misfit dislocations may more seriously degrade the electrical performance of devices built in the layer. The limited stable thickness of silicon-germanium, therefore, constrains the application of silicon-germanium layers. Because very high-performance devices require thin layers (<100 nm) to limit carrier transit times, however, this restriction is not serious. Thin silicon-germanium layers are indeed compatible with device requirements.

The strain in silicon-germanium layers also exhibits the beneficial effect of increasing the energy gap difference relative to pure silicon.[395] For example, while an unstrained silicon-germanium layer containing 20% germanium has an energy gap about 0.09 eV smaller than that of silicon, the energy gap of a strained layer with the same germanium content is about 0.17 eV smaller than that of silicon. The required electrical performance can, therefore, be obtained with a smaller germanium content in a strained, rather than an unstrained, layer.

Carrier mobilities in silicon-germanium layers are expected to differ from the silicon values for several reasons. First, carrier mobilities in germanium are greater than for silicon. Second, the random arrangement of germanium in the silicon crystal structure leads to a reduction in mobility due to an additional scattering mechanism, referred to as alloy scattering. Third, the strain in the silicon-germanium layer modifies the curvature of the energy bands, changing the carrier effective mass and, thereby, the carrier mobility. Finally, the carrier lifetime is strongly reduced due to impurities such as oxygen in the film. Because oxygen is more readily incorporated into silicon-germanium alloys than in silicon, a higher purity ambient is required when forming silicon-germanium alloys compared to elemental silicon films. While most applications of silicon-germanium focus on high-performance transistors, optical devices

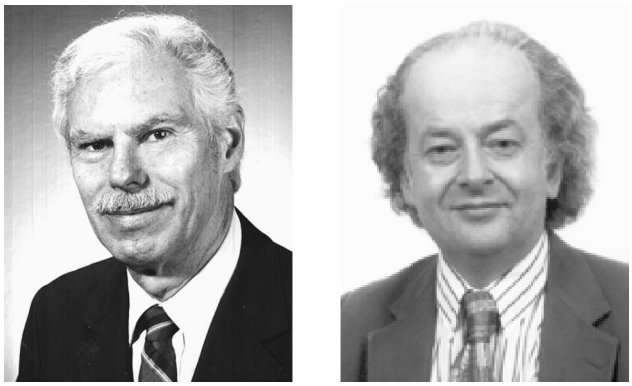

Figure 33. (*left*) Glenn Cullen and (*right*) Federico Capasso.

Figure 34. *Microelectronics Revolutionaries.* The 1998 Silicon Symposium celebrated the 50th Anniversary of the commercialization of the point-contact transistor, and included a special historical session, ''*Fifty Years and Counting*''. Presenters included: (front row, left to right) Norman G. Einspruch, Yoshio Nishi, Bruce E. Deal, S. M. Hu, Junichi Nishizawa, R. C. Newman, and George Rozgonyi; (back row, left to right) Ulrich Gosele, Alfred Seeger, Else Kooi, Jack S. Kilby, Howard R. Huff (Helen Huff, who provided secretarial assistance), Takao Abe, Michael Riordan, Hans J. Queisser, Kurt Hubner, Kiyoo Itoh, and Hideki Tsuya.

may also become important.[393] Because the energy gap of silicon-germanium alloys is smaller than for silicon, the optical absorption edge corresponds to a longer wavelength (*i.e.*, smaller energy) and silicon-germanium is useful as a photodetector at longer wavelengths compared to silicon.

Silicon-on-Insulator

Silicon-on-insulator (SOI) offers the potential for high speed, low-power consumption, soft-error and latch-up immunity, manufacturing process simplification, and smaller chip size. Current SOI manufacturing techniques result in wafers that are more costly than polished or epitaxial wafers. Nevertheless, the benefits often outweigh the higher wafer cost. Some bulk IC designs may be transferred directly to SOI substrates. However, optimization frequently requires mask set and process sequence modifications. In any case, the broad variety of today's IC applications such as MPU's, servers, smart power, RF signal processors require a considerable range of Si-device layer and buried oxide (BOX) layer thicknesses. A number of SOI wafer fabrication approaches are more fully entering into production to serve this range of SOI applications. In that regard, Harold Manaseuit, who received the 1975 Electronics Division Award for his research on the chemical vapor deposition of silicon-on-sapphire (SOS), Katsutoshi Izumi, who introduced the SOI concept in 1988,[396] Jean-Pierre Collinge,[397] P. K. Vasudev,[398,399] and George Celler (Fig. 30), ECS Fellow and Electronics Division 1994 Awardee[400,401] including their colleagues have been long-term proponents of the eventual benefits and utilization of SOI, as has Sorin Cristoloveanu (Fig. 31), the 2002 Electronics Division Awardee and co-editor of the ECS *Silicon-on-Insulator Technology and Devices* proceedings, and his colleagues, who introduced the first double-gate MOSFET in SOI in 1988.[402-404] James Meindl (Fig. 31) has suggested that the double-gate MOSFET with intrinsically doped silicon[405] may indeed be a potential candidate for the end-of-the-roadmap device structure.

Structural and defect characterization of the various SOI wafer fabrication techniques (*i.e.*, bonded, implanted . . .) and correlation among the SOI properties, device characteristics and yield continues to be essential. The relative immaturity of SOI materials compared to polished and epitaxial wafers leads to an additional challenge for the understanding of SOI-specific defects and their impact on device performance and yield in a production environment.

Metrology for SOI wafers is a significant challenge. The particle and site flatness general metrology ITRS characteristics for polished and epitaxial wafers are not applicable for SOI wafers. This arises because interference effects arising from multiple reflections from the Si and BOX layers fundamentally alter the response of optical metrology tools compared to polished and epitaxial wafers, generally degrading the particle measurement capability. The anticipated shift from capacitive to optical measurement of wafer site flatness beyond the 100 nm node may cause a similar degradation of site flatness measurement capability. Metrology methods for many of the SOI defect categories call for destructive chemical etching that decorate but do not uniquely distinguish various types of crystal defects. These defects may not all have the same origin, size, or impact on the device yield, and therefore may exhibit different electrical effects on device characteristics. Nondestructive and fast-turn around methods are needed for the measurement of electrical properties and structural defects in SOI materials.

Nanoelectronics and Compound Semiconductors

The fabrication of artificially structured multielement composites has created new and fascinating devices which may yield the ''transistor of the 21st century.'' These quantum-based devices may be fabricated in multi-layered heteroepitaxial crystalline, disorderd or amorphous III-V compounds and more complicated alloys, which may include crystalline or amorphous silicon and silicides.[101,103] The characteristic dimension of these structures perpendicular to the multilayers is comparable to the wavelength of the carrier transport species, resulting in unique optoelectronic quantum properties. Significant contributions to this arena have been made by a number of outstanding personnel, including ECS Fellows Ben Streetman and Jun-ichi Nishizawa (Fig. 34). Jerry Woodall (Fig. 32), ECS President in 1990-1991, Solid State Science and Technology 1985 Awardee and Electronics Division 1980 Awardee,[406,407] Nick Holonyak, co-author of *Physical Properties of Semiconductors*, in conjunction with Charles Wolfe, Electronics Division 1978 Awardee and Gregory Stillman,[408] Alfred Cho, Solid State Science and Technology 1987 Medalist and Electronics Division 1977 Awardee who established the utilization of molecular beam epitaxy (MBE) for compound semiconductor device fabrication, Morton Panish, Solid State Science and Technology 1979 Awardee and Electronics Division 1972 Awardee,[407] Don Shaw (Fig. 32), Electronics Division 1983 Awardee,[409] Glenn Cullen (Fig. 33), ECS Fellow and Electronics Division 1982 Awardee,[410,411] Bertram Schwartz, Electronics Division 1987 Awardee, S.N. (George) Chu, ECS Fellow and Electronics Division 2000 Awardee, D. Noel Buckley, ECS Fellow and Stephen Pearton, ECS Fellow and their colleagues have played immense roles in the development of these endeavors. The fabrication of artificially structured semiconductors, including the quantum cascade laser, are being developed by Federico Capasso (Fig. 33) and colleagues. They are shaping energy band diagrams to design quantum-structured material configurations to achieve unique device phenomena and characteristics.[412–414] In that regard, Herbert Kroemer has played a most significant role in the science and technology of heterostructures and their applications.

One consequence of this shrinkage of vertical dimensions is the confinement of electrons to such an extent that they no longer exhibit a vertical degree of freedom. The electrons become a two-dimensional electron gas exhibiting very high electron mobilities at low temperatures and unique characteristics. Effects heretofore studied only in basic research projects are becoming realistically achievable and have been discussed, for example, by David Lockwood, ECS Fellow and co-editor of the ECS *Quantum Confinement: Nanostructured Materials and Devices* proceedings, and colleagues. Indeed, spintronics and single electron devices, for example, may offer significant opportunities. One must be cautious, however, to critically assess technological proposals as regards their applicability for both room-temperature operation and for commercial large-scale integration, although selected niche technologies should also be explored.

Quantum interference effects of much larger magnitude are seen even above room temperature in tunneling devices, which operate far from equilibrium. Resonant tunneling diodes exhibit sharp peaks in tunneling current due to the resonant transmission of electrons through quantum well states. Transistors based on this phenomenon have been demonstrated and they may well form the basis for a new scalable IC technology such as the tunneling-based static random access memory (TSRAM) based on the integration of resonant tunneling diodes with heterostructure field-effect transistors providing for fast digital processors with the required large amounts of fast memory ''on chip.'' [415]

Forever Silicon?

The dominant material in the industrial revolution, after more than a century of high volume production, continues to be steel.[416] It was only in the 1920s, however, that the fundamental physical chemistry of steel became firmly understood in terms of its thermodynamic and kinetic properties. At this stage, it appears that we are at a similar stage in the development of our understanding of silicon materials technology. Although crystalline silicon and silicon-based material systems such as Si-Ge have been extensively studied, a thorough description of its material properties is precluded at present due to its extreme structure-sensitivity. The opportunities for further silicon-based IC advancements, including non-planar configurations of silicon ICs, appear boundless, certainly quite sufficient to support numerous research and development thrusts well into the 21st century. Other structural materials, such as Al and plastics, have, of course, entered the mainstream based on their strength-to-weight ratio for structural materials.[416] Similarly, one must be cognizant of paradigm shifts to other material systems for microelectronics, based on the power-delay product, for example, as a useful figure of merit in assessing opportunities for gigascale integration. James Meindl has carefully explicated the trends and fundamental limitations from a systematic analysis for silicon materials, devices, circuits and systems[417] as well as clarify the role of interconnection limitations.[418]

Adventurous technological proposals, however, must be critically assessed as regards their applicability.[419] That is, it is essential to not only understand new technologies, but to also comprehend its impact on the future market structure. Accordingly, development of silicon-based opto-electrotronic systems utilizing porous silicon or alternative quantum-well structures, quantum dots, single-electron devices and other mesoscopic material systems should be carefully assessed as regards their capability of room-temperature operation and applicability for commercial large scale integration applications. Nevertheless, the fabrication of amorphous silicon is an arena of intensive research, affording significant insight into neural networks and thus, perhaps, artificial intelligence. Microclusters, small aggregates of atoms constituting a distinct phase of matter or immersed in a higher-dimensional matrix, may offer unique applications not fully anticipated, especially for a fully integrated silicon optoelectronic system. Additionally, the crafting of molecules and small chemical groups into transistors and related components of computer chips and the appropriate wiring connections has been accelerating. Organic and biological molecules have been identified which can be photochemically ''switched'' in less than 1 psec, comparable to the fastest inorganic semiconductor electronic devices. Indeed, Langmuir-Blodgett organic films or self-assembled monolayers may also be useful in future electronic applications. Furthermore, merging the self-assembly of biological materials with a variety of properties of inorganic compounds (*i.e.*, electronic, magnetic and structural) to develop nanoparticles into macrosized structures has piqued the interest of a number of research and engineering groups.

The drive for efficient photon emission from silicon to develop a low cost silicon-based optoelectronic integrated system has been continuing. The recent compatibility of optically active compound semiconductor materials, such as GaAs, structurally commensurate with silicon materials through engineered interface configurations, may accelerate the fabrication of an optoelectronic system compatible with silicon technology.[420] This combination of gallium arsenide with silicon may be especially important inasmuch as the potential benefit of gallium-arsenide due to its electron mobility of 8500 cm^2/V s has previously been noted to be limited as a result of the thermally limited switching time as well as ULSI system-level limitations such as interconnection resistance.[421] Finally, the development of optical interconnections for a micro-photonic technology would be of immense importance to facilitate the achievement of GHz clock speeds.

Studies in various degrees of research and development including cellular automata, self-assembled structures, fullerenes, carbon nanotubes, metallic clusters in dielectrics and the role of reduced dimensionality in these structures, high-temperature superconductors, optical computers, quantum computers, DNA computers, and other arenas not comprehended as yet, represent areas where major research and selected applications may evolve. In that regard, Carver Mead, 1971 DS&T Callinan Awardee co-author of the widely utilized textbook, *Introduction to VLSI Systems*,[422] may offer

some guidance during his plenary address at the Centennial Meeting of The Electrochemical Society in May, 2002. Indeed, it will be interesting to read the Electronics Division review in 2052!

The phenomenal growth of the IC industry, achieved by staying on the ''productivity learning curve,'' continues to be the gauge by which the industry is measured.[20,22] This is evidenced by the cost per bit or logic function historically declining at ~25-30% CAGR for nearly the past three decades. This growth has been fueled by four factors; shrinking lithographic design rules, yield improvements, increased equipment utilization, and larger wafer diameter. The largest opportunity growth factor to maintain the IC productivity engine and continue on the productivity curve as described by Moore's law[20,21] appears to be increased equipment effectiveness; that is, the percentage of time the equipment is adding value to the wafer. The largest challenge to maintaining the productivity curve, however, may be the enormous financial infrastructure required, rather than technological limits to chip density. In that regard, business and manufacturing ideas will become increasingly important to ensure that the long-term productivity growth of the semiconductor industry maintains its growth near historical levels for the next ten years. More than just monitoring productivity, whether by staying on the productivity curve or increasing manufacturing effectiveness, however, is required. Rather, modeling productivity, the identification of new productivity measures, is required.[423] Global specifications, metrology and standards, in addition to CoO opportunities as discussed earlier, are important mechanisms to ensure the marketplace reality of the ITRS roadmap trends, based on Moore's law, is achieved. The cost effectiveness of international standards for emerging technologies such as SOI and 300 mm diam wafers, in conjunction with the cost-effective production of ICs, such as computer-based design for manufacturability, will offer significant opportunities for an improved quality of life for the world's citizens.

Accordingly, silicon MOSFETs may be expected to scale in an essentially predictable manner from the present state-of-the-art 100 nm technology generation (physical gate length of 45 nm) to the 22 nm technology generation (physical gate length of 9 nm).[22] Nevertheless, the IC industry has continually seen that the ingenuity of device and process engineers to develop unique device geometries, from the early DRAM era[424] and, more recently, nonclassical CMOS devices including vertical transistor configurations utilizing SOI in some cases, double-gate structures with SOI, novel process technologies and models to guide further development may be more influential on IC growth and device performance than might be inferred from extrapolation of today's art and may offer significant unforeseen opportunities.[425–427] The ubiquitous applicability of Si technology in the information revolution, touching numerous aspects of the lives of the worlds' citizens, however, may not necessarily require the state-of-the-art technologies in all applications. It is unlikely, however, that the present worldwide silicon infrastructure will be regenerated to support a silicon successor.[428] Accordingly, silicon technology is expected to continue as the most powerful driver of the information age for at least the next 100 years.

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