3.4 MATERIAL HANDLING SYSTEMS

3.4 MATERIAL HANDLING SYSTEMS

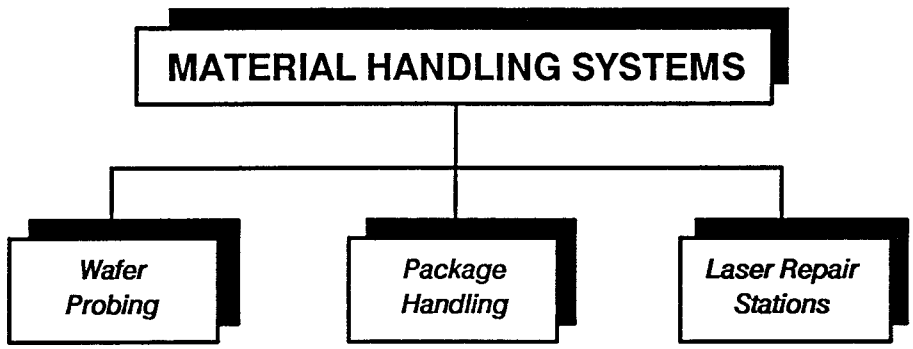
- **The market size was $630M in 1990.**
- **It consists of wafer probers, package handlers and laser repair.**
- **Their 1990 share was 42%, 42% and 16% respectively.**

Material handling equipment serves as a physical, mechanical and electronic interface between test equipment and the device under test (DUT). It consists of three major subsegments commonly referred to as wafer probing equipment, package handling equipment and laser repair systems. (See Presentation 3.4.0-1)

Wafer probers are used to electrically probe dice on an exposed, finished, whole wafer prior to the separation of individual die and their subsequent packaging. Package handlers are used to automatically handle the packaged die. The handler removes each individual die from its shipping tube or container, places it in a test contactor to make electrical connections, and—when testing is finished—puts it in a final bin for further disposition. Laser repair stations are used to increase precision by microscopically trimming resistors, to increase yield by repairing memory elements, and to modify circuits by changing wiring patterns.

At one time this Material Handling Section also included transport and transfer systems for use in the wafer fab area. However, those types of systems have been moved to Section 4.8. They were originally put here because it was believed in the early eighties that as material handling systems became

Presentation 3.4.0-1



Source: VLSI RESEARCH INC
2234-68D

more and more automated they would become the muscle and sinew of a modern factory and develop into a market subsegment of their own. It was believed that this submarket would include material handling systems for wafer fab as well as that for testing. This scenario did not develop as expected, therefore the two segments have once again been separated.

The market for Material Handling Systems relating to test, i.e.—wafer probers, package handlers, and laser repair stations—amounted to just over $400M in the mid-eighties. By 1990 it had grown to around $630M. It is fairly evenly split between wafer probers and package handlers with each holding just at 42% market share in 1990. Laser probers held the remaining 16%.

3.4.1 INDUSTRY CHARACTERISTICS

(Index continued on next page)

3.4.1 INDUSTRY CHARACTERISTICS

3.4.1 INDUSTRY CHARACTERISTICS

- **Wafer Probing is the oldest section–dating back to the late fifties.**
- **Package handling is the most dynamic, due to the advent of surface mount packages.**
- **Laser repair has separated into a separate stand-alone business segment.**

The material handling industry dates back to the fifties and the introduction of the first wafer probers. Package handlers evolved during the sixties as a move away from manual insertion and testing. Laser repair developed in the sixties as well. It was first used for trimming precision components–mainly thin-film resistors in analog circuits. With the advent of memories, low yields demanded that redundancy be used, so a few extra memory cells began to be placed on the chip, laser trimmers were then used to cut connections to the bad cells and rewrite the lines to the good ones.

The material handling industry can be considered to be part of the back-end section of wafer manufacturing, as is test. Most final testing is done in Southeast Asia. Wafer probing is done in either Southeast Asia or at the wafer processing factory, depending upon each company's motivation. As automation has evolved, some probing and even a little final testing, has returned onshore. However, a strong infrastructure still exists in Southeast Asia.

In all material handling equipment, interface to the tester is invariably the main issue. Whether the system is a prober or a handler, it must serve both as a stable mechanical platform which can ensure reliable contacting and as an electrical fixturing tool that will provide reliable high-frequency connections. This places severe limitations on how the equipment must perform; it must be sophisticated enough and robust enough to perform these functions while operating in a very high throughput, rugged, factory environment.

3.4.1.1 Wafer Probing

The wafer probing industry is monolithic, there are no subsegments. However, within the industry there exist three types of probers: those that are fully automatic, those that are semi-automatic and those that are totally manual. Fully automatic equipment loads the wafer from a cassette, aligns it to the electrical probe points that make contact to each die, steps to the die, makes contact and then, when testing is through, returns the wafer to a cassette. Semi-automatic equipment does the same except that it has no facility for automatically loading and unloading from cassettes. The wafer must be manually loaded, but die-to-die stepping is automatic. Manual equipment

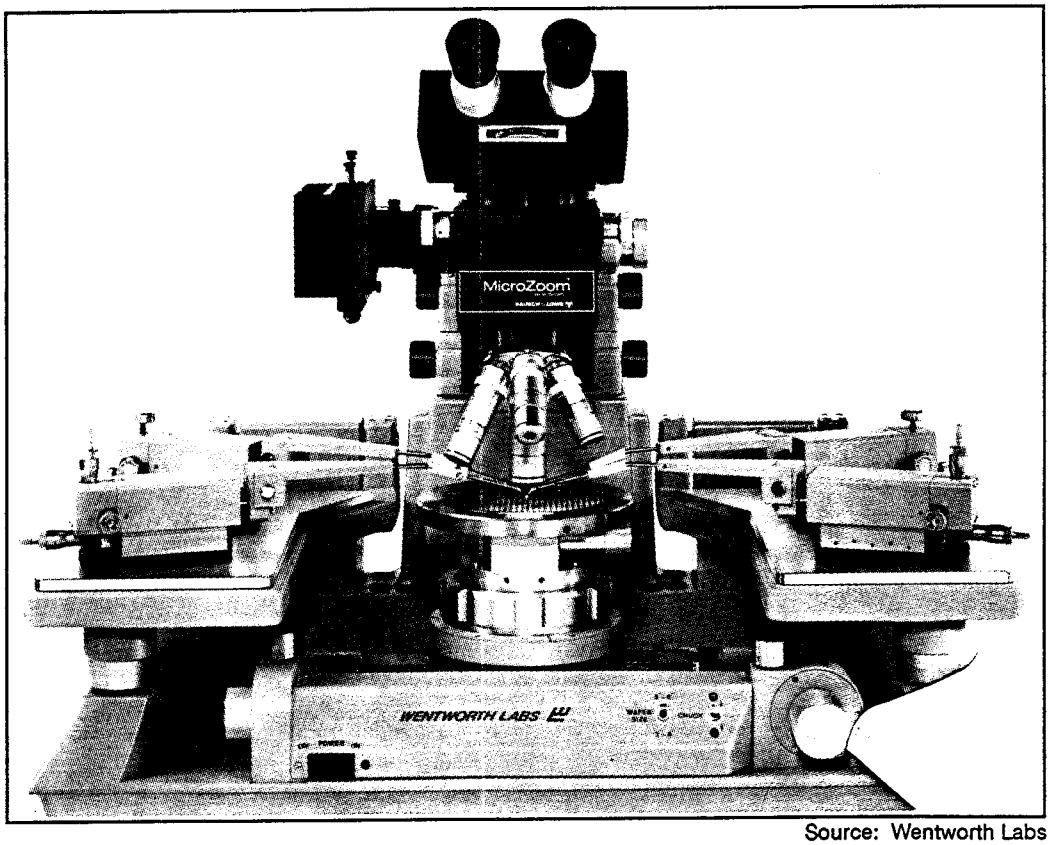
requires manual loading and alignment of the wafer as well as manual die stepping.

Semi-automatic probers typically sold for prices in the range of $30K to $60K in 1990. Fully automatic ones sold in the range of $75K to $120K with some as high as $350K. Manual Probers ranged from $5K to $50K.

3.4.1.1.1 Development of the Wafer Probing Industry

Wafer probing has been an integral part of semiconductor manufacturing for most of the latter's existence. When a component is in need of testing there are essentially two ways to test it, one is to wait until it has been packaged and then test it as a finished part. The other is to test it prior to assembly while each die is still an integral part of the wafer it came from. Economics long ago dictated that testing be done on the wafer. While there are several economic reasons for this, the essential reason is to know that a die is good before adding more value to it.

When wafer probers were first introduced, they were purely manual fixtures that took considerable time to set up and adjust. It is not certain who produced the first ones, but Kulicke & Soffa and Electroglas were among the earliest entrants. Presentation 3.4.1.1.1-1 depicts a modern-day manual prober from Wentworth Labs. While this particular prober was extant in the early nineties, it is nonetheless somewhat typical of the earliest equipment as well.



Source: Wentworth Labs
2234-70

Presentation 3.4.1.1.1-1

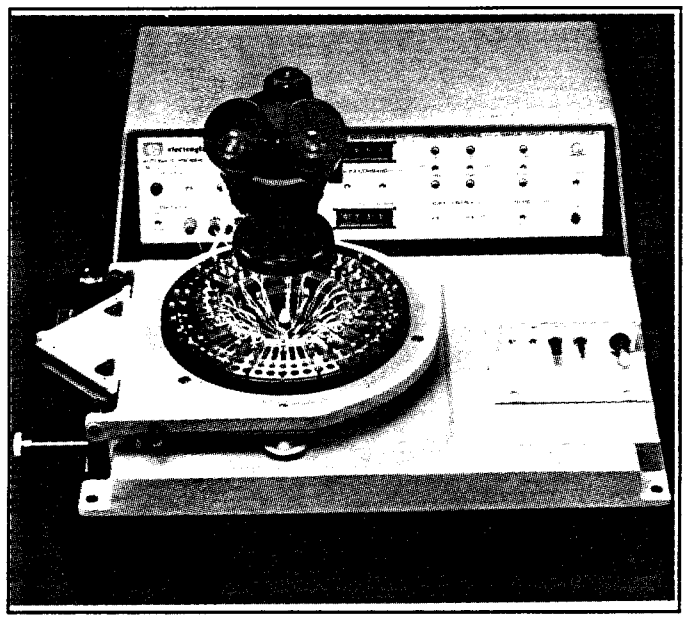
A Wentworth Labs manual prober

The important elements of a manual prober consist of a microscope for viewing a die on the wafer during positioning, a chuck to hold the wafer, two micromanipulators to move the chuck and the wafer in unison in a horizontal plane called the X-Y plane, a platform to hold other—smaller—three dimensional micromanipulators which themselves hold needle-like probes to contact the die pads on the die, and finally a third Z-axis micromanipulator for rasing the chuck and bringing the die into contact with the electrical probes.

Wafer probing is quite an involved activity, requiring three mechanical degrees of freedom for the wafer and three-times-N mechanical degrees of freedom for the probe points. N represents each electrical contact that must be made by one of the N probes. Setup times can sometimes take hours, for each contact has to be precisely positioned in the XYZ planes. Subsequently, great care needs to be taken, for any slight slip can dislocate one of the contacts, resulting in scratched films on subsequent dice probed, or no contact to the die. Either results in the throwing away of perfectly good dice. Wafer probing is therefore an ideal activity for automation and, in fact, became one of the earliest manufacturing activities to be automated.

The first semi-automatic prober was introduced in 1964 by Electroglas. This occurred at WESCON in Los Angeles, as SEMI had yet to be founded. An example of an early derivative of that first Electroglas semi-automatic prober is shown in Presentation 3.4.1.1.1-2. The semi-automatic prober was quite an advancement for its time. The wafer chuck was mounted underneath the frame (and can no longer be seen) where it moved on two screws perpendicular to each other. These screws were, in turn, attached to stepping motors which could automatically step the wafer die-by-die completely across its surface within the X-Y plane, much as modern day lithographic steppers do. The wafer prober platform was, in fact, the forerunner of modern day stepper platforms.

The system was designed so that X, Y and Z movement of the wafer chuck could be programmed by manual entry. The X/Y movement was accomplished via stepper motors as mentioned, the Z movement was accomplished via a plunger which simply raised the chuck a certain predetermined distance upwards. The individual probe point positioners were now mounted on a platform which could swing away, as seen in the picture. This mitigated the need for individual adjustments. Also note the small screw foot at the front lower part of the platform. This became the micromanipulator to adjust Z-axis distance, but it was now



Source: Electroglas
2234-71

Presentation 3.4.1.1.1-2

Model 901 automatic wafer prober by Electroglas

mounted on the platform, not upon the chuck.

This system required four new design features in order to work appropriately. One was the ability to sweep the chuck forward and out from under the platform so that wafer loading and unloading could be accomplished. Another was the need to be able to receive a signal from the tester, telling the prober when to index the wafer to the next die. The third was to be able to detect the edge of the wafer and step forward to the next row of dice. The fourth was to be able to receive a failed signal from the tester and automatically mark the bad die with red ink.

These were major improvements. Other manufacturers soon followed with similar systems. By 1970, Pacific Western Systems and Teledyne TAC had become the second and third tier leaders just behind Electroglas.

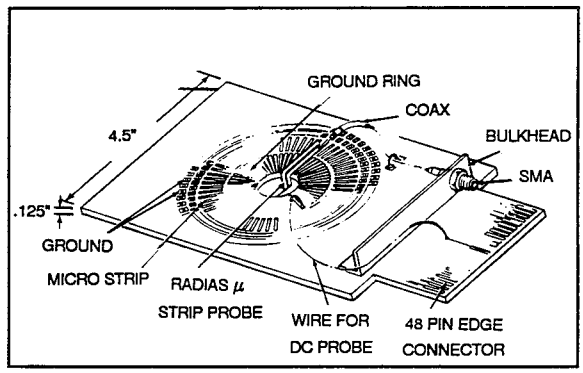
Still, wafer probing suffered from use of a single micromanipulator for each pad. Setup time remained unduly long. Moreover, it was not possible to test die at very high frequencies for the connecting wires were still too long. Finally, it was not easy to connect the tester to the probe wires. Further improvements were still needed.

It was soon to be discovered that another subtle but dramatic advancement had been made in this system which was to pave the way for modern high-frequency probers. That was the unique mounting of the prober micromanipulators. For rather than being mounted individually on the major movable platform, they had been mounted instead on a so-called single fixture called a 'probe-ring' fixture. This fixture could be rotated on two axes—the Theta and the Phi axes—allowing simultaneous positioning of all probe points relative to the die pads. Once this concept of probe-movement-in-concert was recognized, the development of probe cards soon followed. These would prove to provide a stable mechanical platform, an immensely reduced setup time, and the ability to test unseparated die at previously unheard of frequencies.

A small company called Rucker & Kolls invented the first probe cards. They accomplished this by cutting a hole in a conventional printed circuit card that was itself designed to plug into a standard printed circuit card socket. They then individually epoxied each of the probe points directly onto the printed circuit card. While the epoxy was still wet, the probe points were microscopically positioned on a mylar reproduction of the actual die.

In this manner the probe tips were precisely pre-positioned in the X and Y planes and were 'planarized' so that they didn't stick up or down into the Z plane. In one stroke this advancement reduced setup time to a few short minutes, increased the potential operating frequency still further by a wide margin, and provided a stable platform to which the large, heavy, test head could be docked without crushing the tiny probes.

A drawing of a probe card is shown in Presentation 3.4.1.1.1-3. This particular card is manufactured by Cerprobe rather



Source: Cerprobe
2234-72

Presentation 3.4.1.1.1-3

A Cerprobe probe card

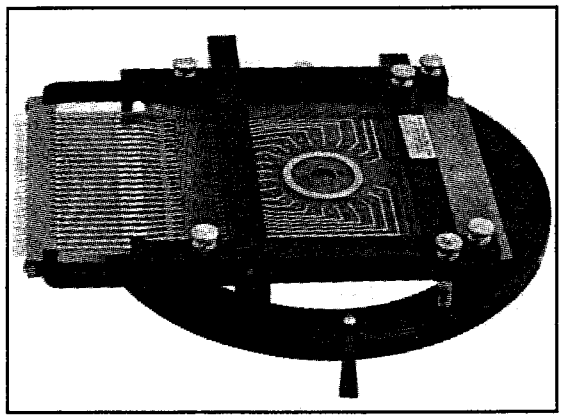
than R&K. It does not use the epoxy ring method of R&K, but it does show more clearly how the card is configured. Presentation 3.4.1.1.1-4 depicts a card mounted in its probe ring. In this case the picture is of an early R&K card and its probe ring mount. The screws which allow X,Y,Z, theta and phi prepositioning can be clearly seen.

The total high-frequency interface between tester, probe-card and prober is depicted more clearly in Presentation 3.4.1.1.1-5. In this instance the drawing depicts a round probe card rather than a square one. The Tektronix test head is shown in its vertical position, which is normal before docking with the prober. The fixturing is shown exploded above the Electroglas prober.

In the early seventies another company, called Xynetics, developed a linear reluctance motor which provided improved speed over the X/Y lead screws. This motor was adapted by Electroglas for its probers. Xynetics ultimately acquired Electroglas and for a while downplayed the Electroglas name. Both companies were subsequently acquired by General Signal. R&K, too, was acquired by General Signal, but was eventually divested in 1990. A drawing of a fully automated Electroglas Model 2001X is depicted in Presentation 3.4.1.1.1-6.

Electroglas, though early in the market, did not actually provide the first fully automated wafer prober. That honor went to Cobilt. The turn of events with Cobilt are very interesting and lead into the modern-day industry.

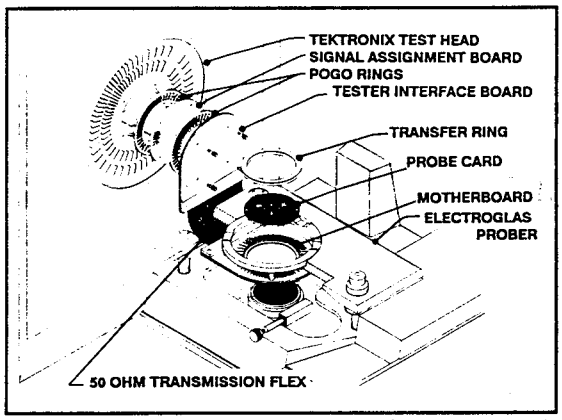
Cobilt started in the early seventies as a probe card manufacturer, but then soon branched into the prober market itself. It began to supply fully automated probers in 1976 as custom-built systems for IBM. These custom-built systems did quite well but floundered commercially because they were too expensive for the time. The CP440



Source: R&K
2234-73

Presentation 3.4.1.1.1-4

R&K Model 107 probe card adapter

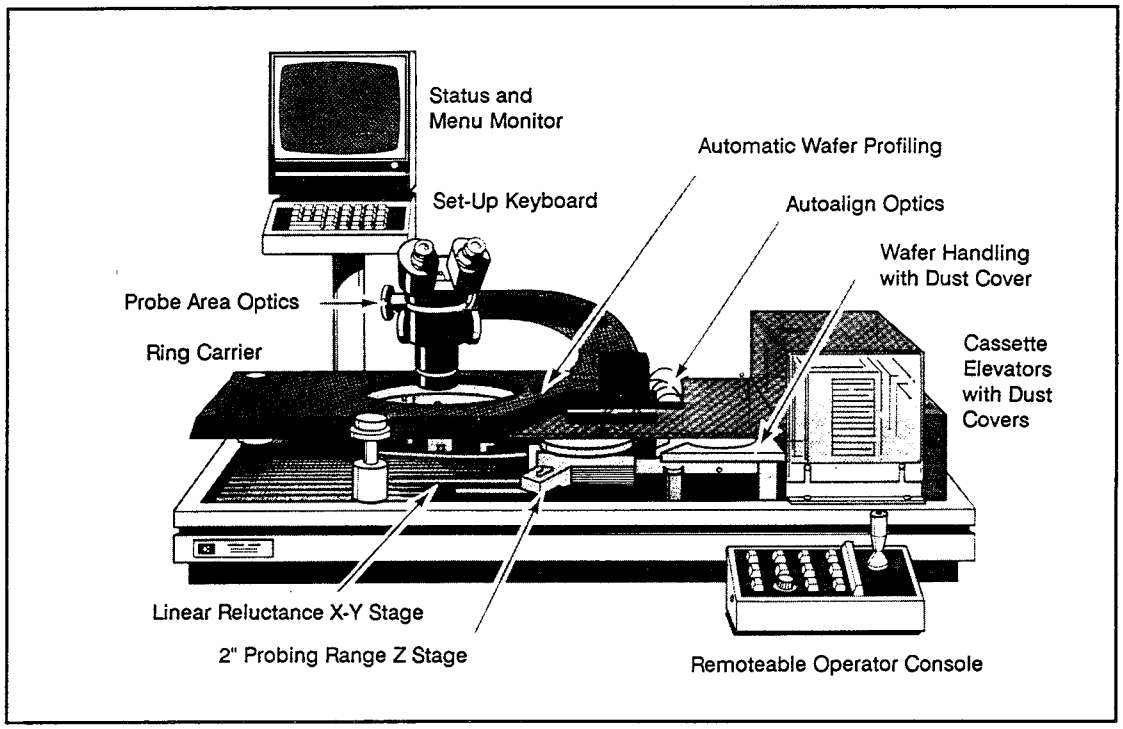


Source: Tektronix
2234-74

Presentation 3.4.1.1.1-5

A Tektronix to Electroglas interface

commercial version sold for $70,000 at a time when semi-automated counterparts were around $20,000. In 1977 Cobilt sold the rights for its manufacture in Japan to its Japanese representative TEL (Tokyo Electron Ltd). This machine was ideally suited to the more expensive Japanese approach to improved reliability and quality through full automation. TEL set about restructuring the machine for the Japanese market. First



Source: Electroglas
2234-75

Presentation 3.4.1.1.1-6

General Signal-Electroglas 2001X wafer prober

it translated the manuals into Japanese. Then it began replacing piece parts item-by-item with Japanese components, until the machine eventually became a Japanese look-alike of a previously All-American version. This new machine achieved instant, and virtually overwhelming, success in Japan. In 1979 TEL offered it back to Cobilt as a reverse re-license to the American market as the CP4400A. This machine was one of those which was to propel TEL to the number one market spot in all semiconductor equipment in just a few short years.

In 1981 Applied Materials acquired Cobilt and authorized another redesign of the CP4400. This was to become the AM4500 prober (or the CP4500). It was subsequently sold to Eaton who renamed it the Autoprobe 2000. It reentered the industry in 1984 as the Eaton Autoprobe 2000. This occurred just at the peak market growth year of all time, and just prior to 1985, the year of the most precipitous market drop of all time. Eaton had banked on 1984 being typical rather extraordinary, and could not adjust to the 1985 drop. It exited the market in 1986, having sold the Autoprobe 2000 to KLA. There it was resurrected one more time as the KLA 1007. KLA subsequently used that design as the stepping stone for a complete set of fully robotic systems and is today quite successful in their sales.

Meanwhile, Pacific Western and Teledyne TAC gradually lost market share to these leaders. In those early years, virtually every manufacturer who introduced a fully automated prober into the American market experienced problems. Electroglas introduced the model 1038X in 1977. It was eventually pulled from the market.

Electroglas was preparing a still newer entry which would be successful. It was the 2001 series machine. During its redesign Electroglas paid great attention to providing unusually high-uptime. The machine proved to be as good as any Japanese product, allowing Electroglas to regain much of the previously-lost market share.

Teledyne Tac followed a similar route but with less visible success. It introduced the fully automated Model 710 in 1979 or 1980. The design proved cumbersome and unreliable. It was pulled from the market and reintroduced in 1981 after redesign. A third model, the 823 was subsequently introduced. In 1991, Teledyne TAC exited the market.

Pacific Western announced a fully automated prober in 1980. It was called the model SP3. Subsequently, it introduced a model, named the Probe II, and then the Probe III. None permitted PWS to regain its lost market share.

In Japan, a company called TSK, Tokyo Seimetsu Co. Ltd., produced a new prober which could literally be set up and then left on and virtually forgotten for the several days that probing of a box of cassettes took. This propelled TSK into the front ranks along with TEL. Advantest chose to favor TSK on its automatic testers, giving the company a substantial edge. The product was marketed outside of Japan by Advantest.

3.4.1.1.2 Application Technology of Wafer Probing Equipment

While much of the application technology for wafer probing equipment was developed in the seventies and the eighties, there are still several new areas that continue to develop.

Some issues which have been in the making for some time, but which still generate new applications technology consist of parallel probing, off-line inking, die pad size, pin count, and hi-volume versus hi-pin-count probing. Other emerging issues are clean room probing, reduced quantity of probing with increasing yield, and more reliable high-frequency probing.

Among these, a key issue driving most of these is the trend towards a higher lead count. Rent's rule relates the quantity of leads to the number of gates. Rent's Rule is merely a statement to the effect that lead count for logic circuits will increase proportional to the square root of the number of gates in the circuit. This follows naturally from plane geometry. For each 100,000 gates, there will be 320 leads, more or less. The actual value is dependent upon a multiplicative constant which will increase or reduce this number.

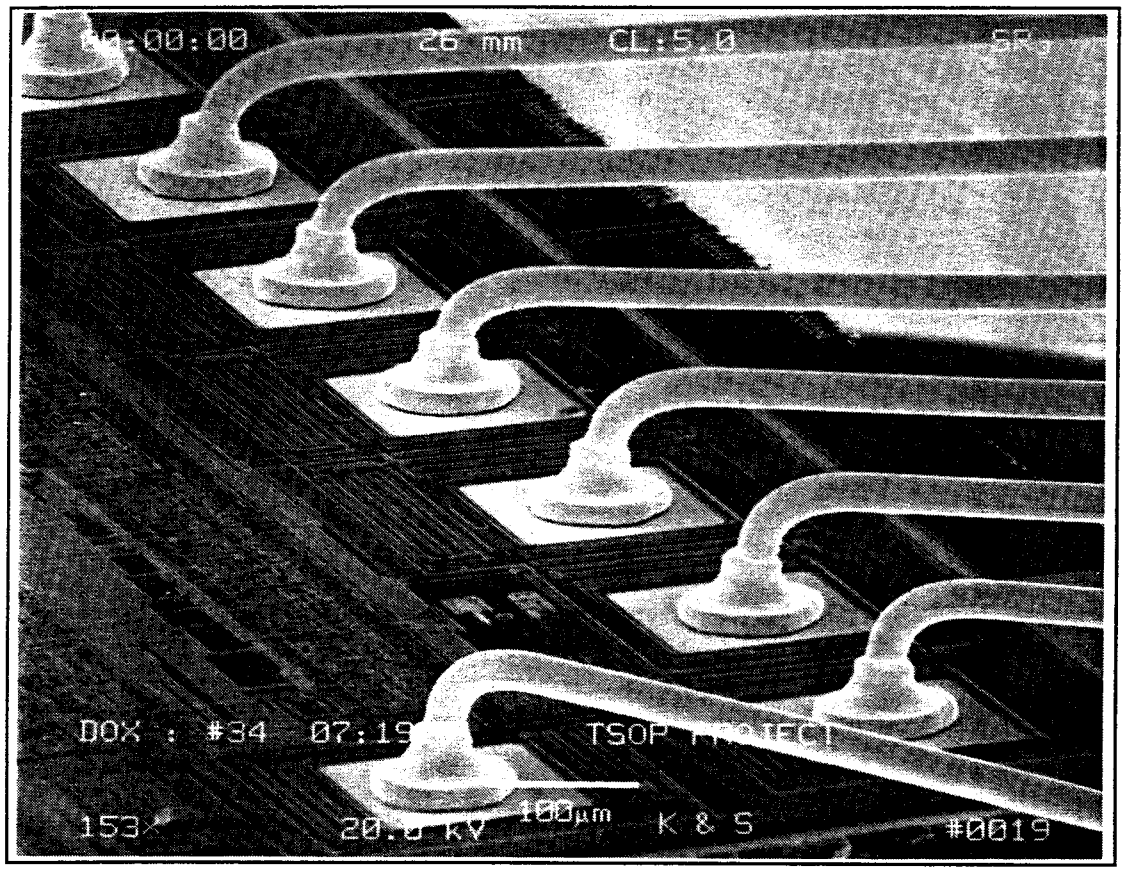
Lead count—or pin count, since the two terms are used synonymously—affects pad size, probe point count, parallel probing, frequency and volume. There is a disparity, however, between IC manufacturing and the equipment design to accommodate pin count. By far, the largest quantity of IC products have 64 leads or less. This can be seen by examining Table 1.9.2-4 which appears in Section 1.9 of Volume I. A brief extract of that data is depicted below in terms of millions of packages used in 1990, as well as projections for 1995:

IC pin count	*1990*	*1995*
11-16	25,400	28,300
17-24	10,700	17,900
25-40	6,500	11,100
41-64	2,600	7,500
65-96	3,100	9,800
97-256	1,700	9,000
>256	300	3,900

The greatest pressure in terms of volume of manufacturing is clearly for the low pin-count devices. Still, test and probe equipment must be manufactured to meet the

highest pin counts to be encountered, not the average volume. Therefore, a disproportionate amount of cost of the prober must go into accommodating high lead count dice.

From the IC supplier's vantage point, the manufacturing issue of increasing lead count is one of a trade-off between the cost of silicon and the reliability of smaller wire pads. This is made more clear by Presentation 3.4.1.1.2-1. This is a photomicrograph of wires attached to bonding pads in a modern TSOP package. Note that the pad size is about 100x150 micron. This is equivalent to a 4x6 mil pad. The distance between pads is roughly 4 mils as well, and the total pitch is about 8 mils. A substantial amount of silicon area is taken up for pads. It would be desirable to reduce pad size. However, the photo also shows the reliability side of the issue. Each wire-bond to a pad can be seen to take up about three-fourths of the pad area. Room must be left for the pancaking effect of the wire bond. Only about one mil remains on each side for bonding error. The specific wire-bond in the picture that is on the pad nearest the upper left hand edge can be seen to be just barely inside the pad boundary. Most wire-bonding equipment has a tolerance margin of about one-half mil or more. Wire bond suppliers say that smaller bonds and tighter tolerance bonds can be made, but the cost



Source: Kulicke & Soffa
2234-76

Presentation 3.4.1.1.2-1

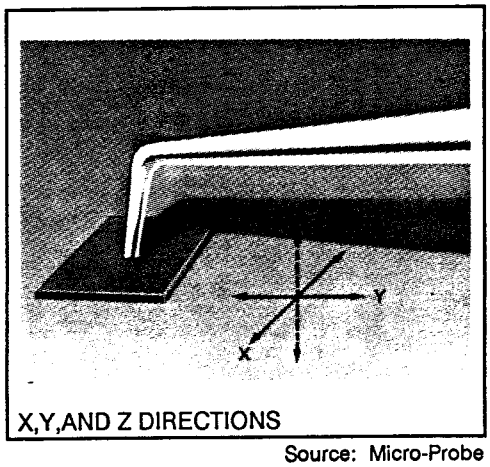
Photomicrograph of high lead count device in a modern TSOP package.

is out of reach at present. Still, IC suppliers are cutting down on the pad size. Pad pitches of 6 mils are becoming quite common, with 4 mils for the pad and 2 mils separation. Some IC houses say they would like to go to a 3 mil pitch, but to our knowledge there are no wire bonders that can yet match this.

Such a 3 mil pitch on a high-pin count package will likely cause probe costs to skyrocket. This will be particularly true if parallel die probing continues. At present, parallel die probing is almost exclusively used with memory devices where extremely high volume and low pin count permit more efficient operating approaches. However, if parallel probing begins to be performed with high pin count devices, new probe methods may be needed.

Another issue with high pin count is the force applied to the wafer and the prober. This begins to become excessive with such high pin counts. Moreover, the permissible tolerance on each probe point tightens excessively. Presentation 3.4.1.1.2-2 depicts a typical probe tip in contact with a probe pad. In order to assure that good electrical contact is made, the tip is usually 'scrubbed' into the surface. The typical scrubbing force is about 3 to 5 grams per point. This is small enough for a single tip, but as can be seen in the table below, scrubbing pressure for the entire set can become excessive. The end result is a need for still more ruggedized equipment capable of withstanding such enormous pressures while holding the numerous probe points to within a few microinches.

Lead Count per Die	*Number of Die Probed in Parallel*	*Total Probe Pins*	*Scrubbing Pressure on the Die, Wafer and Chuck @5 gms per point*
20	8	160	0.8 Kg 1.8 lbs
20	16	320	1.6 Kg 3.9 lbs
80	8	640	3.2 Kg 7.1 lbs
80	16	1280	6.4 Kg 14.1 lbs
240	8	1920	9.6 Kg 21.1 lbs



X,Y,AND Z DIRECTIONS

Source: Micro-Probe
2234-77

Presentation 3.4.1.1.2-2

A typical contact between probe point and pad.

Z-stage strain, which effectively causes gouging into the die, is typically 5 to 10 microns per pound. A 10 pound load can cause upwards of 100 micron strain, enough to destroy a die. X/Y stage slip due to heavy loads can also be about the same amount. When expressed in inches, this is 0.1 to 0.2 mils displacement per pound. A 10 pound load may cause slip of as much as one to two mils. This may be excessive for large die with 3 or 4 mil pad pitches.

Turning now to a different topic, off-line inking has been a requirement for several years. The high cost of test & prober equipment coupled to the slow speed and cumbersomeness of on-line inking has caused the use of delayed off-line inking. In this

instance, a stored record is made of the location of the good die during test. Later the stored data is used to ink the bad die on another prober set up off-line for just that purpose. The typical ratio of prober use for off-line inking relative to that for on-line testing is between 1:5 and 1:10. Consequently, one can expect that about 5 to 10 percent of the prober market will be for off-line inking.

Off-line inking is dominantly an alternative adapted by those companies who use outside assembly houses or somewhat non-automated die bonding. The reason is that the data which identifies the good die on the wafer is kept in a computer database. It can be kept as easily as not in the company's host CIM system and transported to the point of use if the company does its own probing. So, if the end point of use is a die bonder within a factory belonging to that user, there will be little need to ink the die. Rather the bad dice can be identified from the database and simply ignored at the pick & place activity at die bond.

However, since all companies will at one time or another experience factory overloads in bonding, they will also at one time or another have need of some off-line inking at outside houses. Consequently, even in those companies who do their own packaging, there will usually be at least one off-line prober that is kept as insurance for those inking requirements.

Clean room probing began to become an issue about five years ago. Currently most probing areas that are 'clean room certified' appear to be about class 1000 or above. Clean room probing is not needed for the die itself, because by that time the wafer will have been passivated and will be reasonably immune from the particulates encountered in wafer fabrication. However, the wafer is still susceptible to particulates and contamination on the pads themselves and in the packaging. Consequently, while more clean room probing is being performed, the clean room requirements are not as strenuous as in wafer fab. Still, this will have a substantial effect on new equipment design.

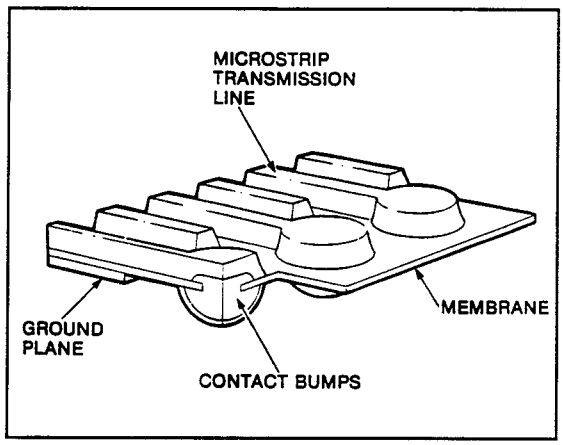
More reliable high-frequency probing also continues to demand attention. With probe cards, the upper frequency limits appear to have been reached. TI & AT&T manufacture some probe cards for RF probing. Logic testing, however, is limited because of the inability to tune the circuit and match impedances. Transmission lines can be used on the probe card itself, but not much can be done from the probe point to the die pad. Tektronix and Hewlett-Packard have developed membrane probe cards which solve this issue and do permit higher frequency probing, well into the gigahertz region. Unfortunately, neither Tektronix nor HP are in the prober business.

Membrane probing is an issue that may well make or break the American Prober Industry. This is because high frequency probing is a problem that is very much imbedded in the heart of the prober and is viewed as a probing problem by the customer. Unfortunately, most American prober suppliers view it as a probe card issue rather than as an equipment issue and therefore as not being their problem. Japanese suppliers, however, see it as a solution to a customer's problem and takes ownership of the issue. For that reason, an acceptable improvement in the design will likely come from a Japanese supplier rather than from one of the American suppliers and will likely result in loss of market share by U.S. suppliers. This is exactly what happened with the photoresist market place and the IC packaging marketplace.

The membrane probe card consists of a flexible dielectric membrane which supports a microstrip transmission line. It permits a complete microstrip transmission line to exist from the ATE test head right to the

pad itself on the die. A drawing of the Hewlett-Packard probe is shown in Presentation 3.4.1.1.2-3. Conceptually, the location of the bumps on the membrane are patterned to match the pads on the die. The flexibility of the membrane permits a hammer head to be positioned above the membrane. The hammer head pushes down upon the membrane, flexing it and forcing it into contact with the die. Upon release, the membrane then returns to its original position above the die. Presentation 3.4.1.1.2-4 shows a cross-section of the membrane card. As of this writing, the membrane card has proven too expensive to put into every day practice except for UHF frequencies and beyond.

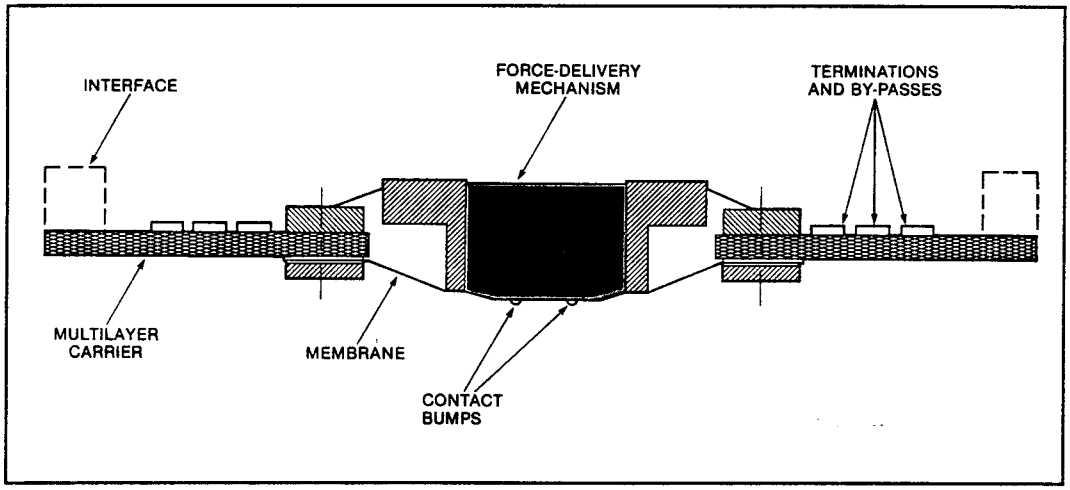
Other emerging technology issues dealing directly with the equipment are probe-mark inspection, automatic probe to pad alignment, automatic probe card changing via cassettes, and equipment modification for operation in the clean room.



Source: 1988 International Test Conference, P. 601
2234-78

Presentation 3.4.1.1.2-3

The membrane probe method



Source: 1988 International Test Conference, P 602
2234-79

Presentation 3.4.1.1.2-4

Cross section of the membrane probe

Among these, automatic probe-to-pad-alignment and probe-mark-inspection is being addressed via pattern recognition methods already developed for automatic alignment. Automatic probe card changing is a mechanical positioning and placement issue concerning how to swing the card beneath and around the probe card ring and platform without interfering with the chuck or the wafer cassette rack. This will likely be solved relatively easily once enough demand exists to justify it. This will likely come from ASIC houses where fewer than six wafers per lot are usually tested.

Equipment operation for the clean room will require major rethinking of the prober. Intake and exhaust cooling air inlets will be needed. At the minimum, all exhausts will need to be directed downwards. Polymers and oils that are normally used to move the prober will need to be replaced with oilless gears and bearings. Moving metal parts will need to be replaced with material that does not throw off metal particles. Cabinets will need redesign. For example, it has been shown that the removal of one #10 sheet metal screw throws off more than 10,000 heavy metal particles. This will need to be eliminated.

3.4.1.2 Package Handling

The package handling industry splits along two directions. One leads to a bifurcation according to the type of package mounting scheme—whether it is to be surface mounted or through-hole mounted. The other leads to a separation by type of package—DIP, LCC, Transistor, small-outline, etc. In the past, VLSI Research has classified handlers by the latter. However, we have more and more begun to classify by the former because the entire IC industry has begun to categorize packaging as either surface-mount or through-hole mount.

3.4.1.2.1 Development of the industry

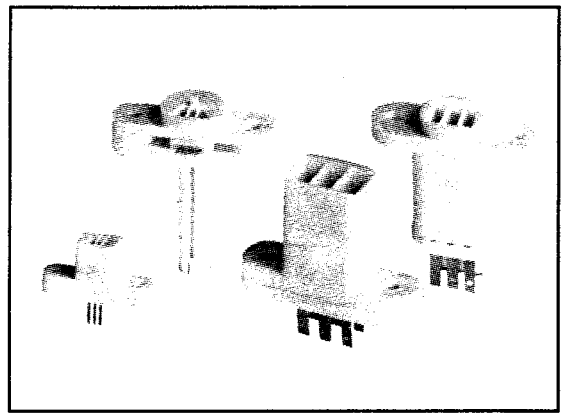
Handling equipment, or more properly package handling equipment, evolved during the sixties in a period when manual handling of devices was becoming impractical. Prior to this, packages were manually inserted into a tester by a production operator. In fact, during this time the tester as it is know today had not yet developed. Most testing was done using a curve tracer. During this period of development most of the effort was being placed into making sockets which were easier to manually insert the device into, and in making fixtures which could support all the cabling and routing for extra wiring to connect to other power supplies, meters and generators.

Manual insertion was limited to the speed of the operator. This typically ranged from between 300 units per hour on the low side to nearly 500 units per hour on the high side. Cost was not so much of an issue back then as was accuracy and demand. Transistors were selling for a low of about three dollars to a high of several hundred dollars. The hot item of the day was the 2N706 transistor which sold at $75. Operators typically were paid $3.50 an hour in the United States. Even with overhead burdens as high as 700%, the slowest and most costly operator still only added about nine cents to the cost of manufacturing. However, yields were low and error rates were high. Consequently, many good parts were being thrown away as being bad, while many bad parts were passed on the customer as being good. Automatic test equipment was coming into being to replace the operator's

judgement, but nothing was replacing the errors in insertion, such as undetected bent leads, etc.

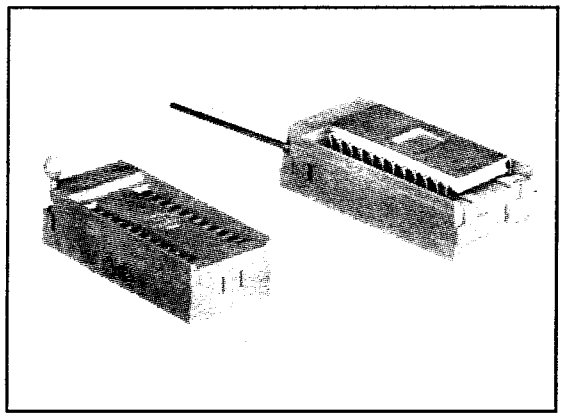
Flared sockets and zero insertion pressure sockets (ZIP DIPs) such as shown in Presentation 3.4.1.2.1-1 came into being to offset this slow speed and high insertion error rate. Carriers came into use for fragile-pin devices such as flat packs and 8 or 10 lead top hat packages. Carriers surrounded the device and contained the leads individually in three-sided trenches or wells where they could be well protected. Such sockets and carriers are still in widespread use today for engineering and other manual applications, but they are discouraged as much as possible in production, for the device must be first inserted into a carrier before it is tested. It must then be removed from the carrier just prior to shipping. With the emergence of very fine pitch packages which are very costly, there has, however, emerged a new tendency to return to the carrier as a means for protecting the component.

The earliest handlers were the so-called bulk-feed handlers. These often looked somewhat like a cream separator such as used to separate cream from milk. Presentation 3.4.1.2.1-2 depicts a Daymarc IC handler from the mid-sixties. Devices were dumped into the large bowl-affair standing separately from the handler itself. The bowl, known as a vibrator, shook rapidly and forced the devices to gather along the outside rim and onto a specially designed railing. As they moved along the railing, the rail passed through various contortions designed to cause mis-aligned devices to fall back into the bowl vibrator, while properly aligned devices continued to wind their way along and eventually into the thin connector tubing which acted as a conveyor track. Gravity did the rest, the aligned device would fall onto a 'singulator'. This was a mechanical gate that would let only one device at a time pass, as needed, and at the correct time. From there it would fall right into the handler mechanism.



Source: Textool

3 lead in-line test sockets



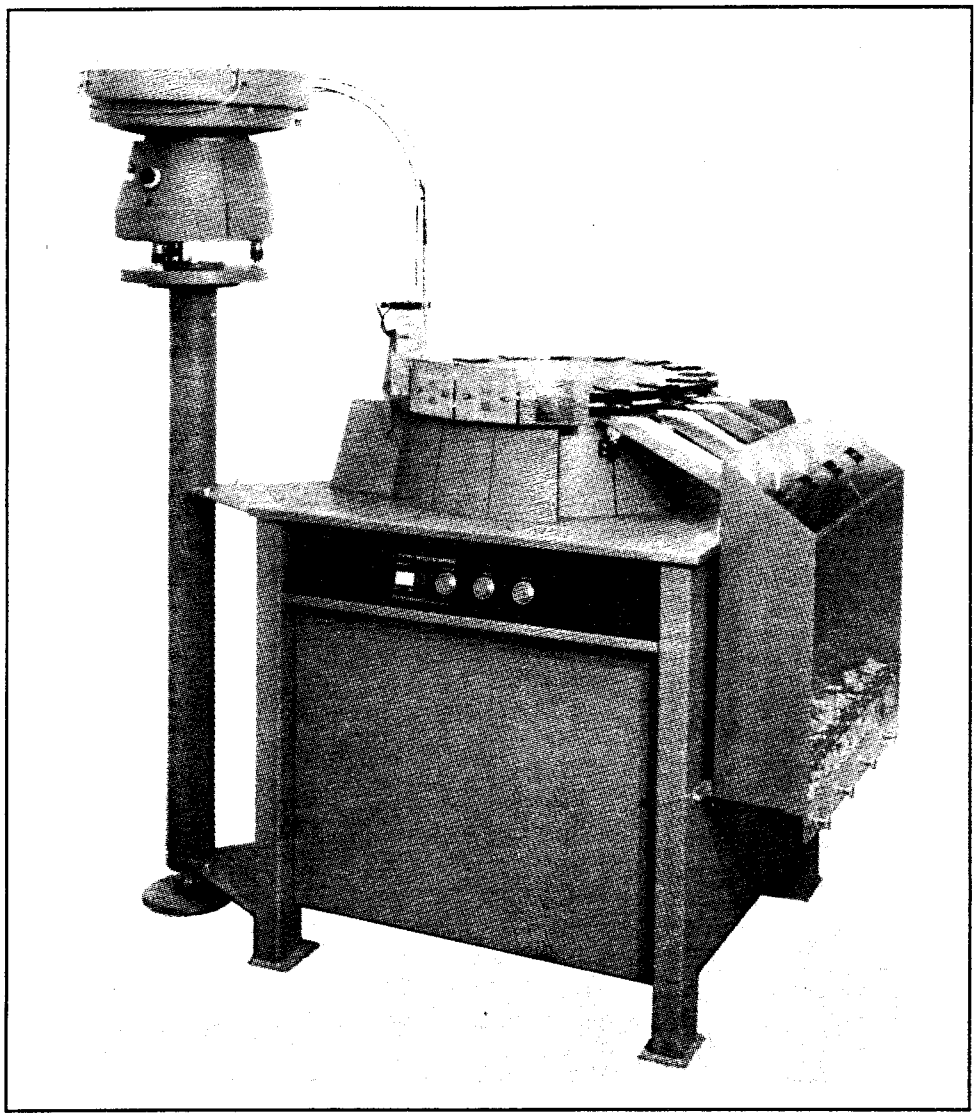
Source: Textool
2234-80

Zero insertion pressure (ZIP DIP®) sockets

Presentation 3.4.1.2.1-1

Test Sockets for manual insertion and handling.

There, the device comes into a so-called contactor which performs both mechanical alignment and electrical connection. In addition, the contactor represents a thermal mass which will keep the device—now called the device-under-test or DUT—at whatever temperature it is being tested at. A typical



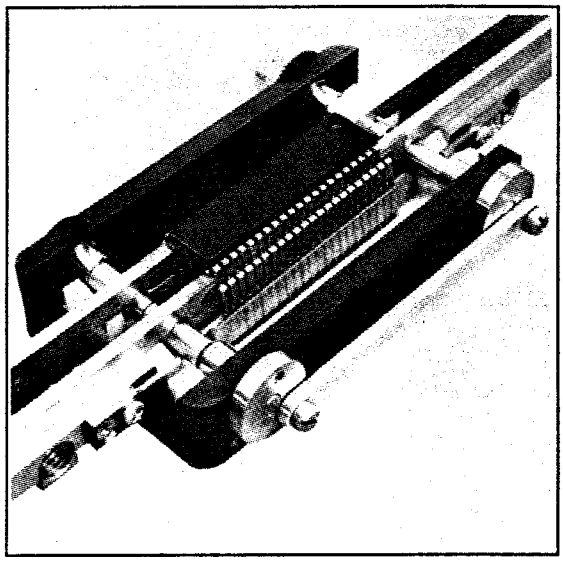
Source: Daymarc
2234-81

Presentation 3.4.1.2.1-2

An early IC handler from Daymarc

contactor from an early machine of 1975 vintage is shown in Presentation 3.4.1.2.1-3.

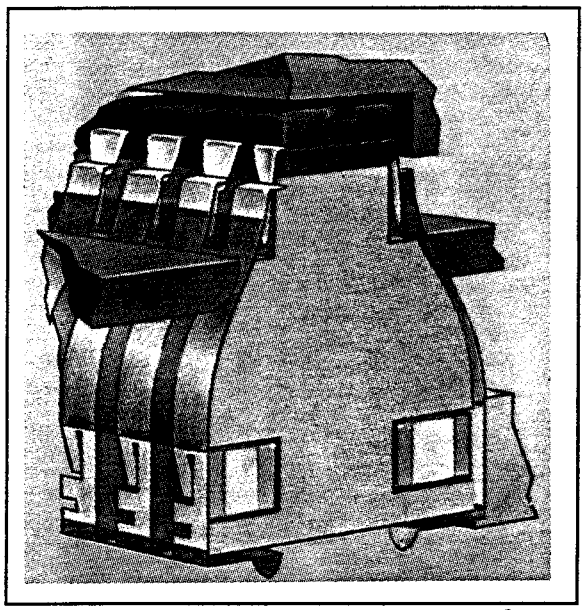
The contactor railing that the DUT rests upon is part of the conveyor assembly that brings the DUT from its bowl assembly or shipping tube to the contactor mechanism. A second mechanical lever stops it at the proper position. There, a set of contacts that are almost mirror images of the pins of the DUT wait to be spring-loaded into contact with the pins. Each pin of the DUT is gripped between these articulated spring contacts. They connect electrically to the test circuit. A close-up drawing of a modern-day contactor supplied by Sym-Tek is depicted in Presentation 3.4.1.2.1-4.



Source: IPT
2234-82

Presentation 3.4.1.2.1-3

Contactor Assembly



Source: Sym-Tek
2234-85

Presentation 3.4.1.2.1-4

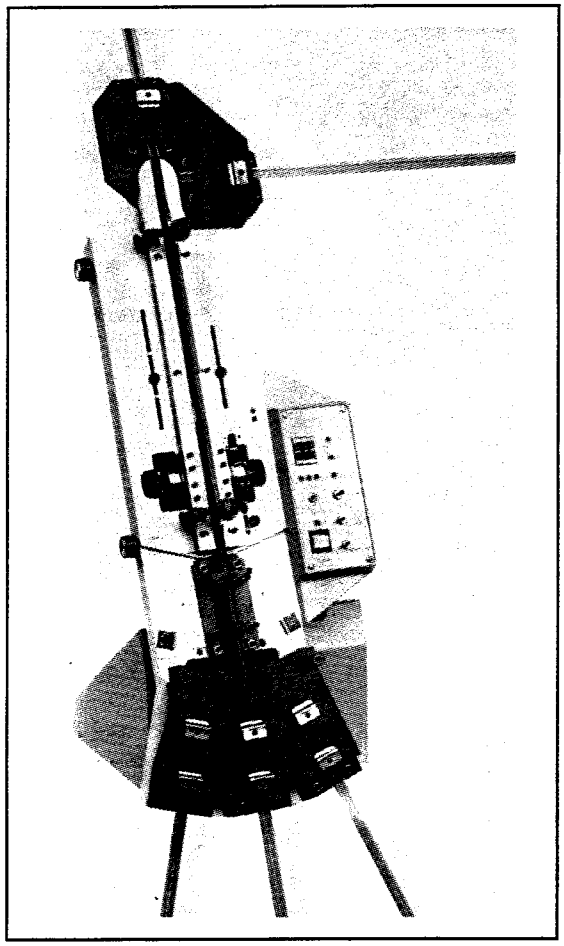
Drawing depicting a DIP contactor on a Sym-Tek MTS handler.

The contactor became one of the more critical aspects of handlers since it had to be mechanically rugged, to be of long life and able to withstand the high abrasiveness of the DUT, to be of sufficient thermal mass to maintain constant temperature, to be an electrically stable platform that would enable relatively high frequency testing, and all the while to have electrical contact springs that could perform millions of flexures back and forth without breaking, losing electrical contact or mechanical integrity. This was a tall order, so for many years the contacter was the key strategic element-of-success among handler suppliers.

Once a device has been completely tested, a signal from the tester signals the handler that it is finished and whether the DUT passed or failed. The tester also grades the DUT by category of goodness or badness and sends a signal to the handler to tell it which bin to drop the part into. These bins can be seen back in Presentation 3.4.1.2.1-2 as bulk bins which the completed devices are dropped into.

This methodology proved quite successful; the earliest handlers could manipulate devices more than ten times faster than could an operator, thus bringing testing into the range of 4,000 to 7,000 units per hour (UPH). Modern handlers range from a low of some 2,500 UPH to above 25,000 UPH.

During the seventies, handlers subsequently developed along two other lines, that of being either very sophisticated general purpose production testers with numerous binning capabilities, or that of being inexpensive bench-top handlers for non-production purposes. An inexpensive handler is shown in Presentation 3.4.1.2.1-5 while a very expensive high-speed system is shown in Presentation 3.4.1.2.1-6.



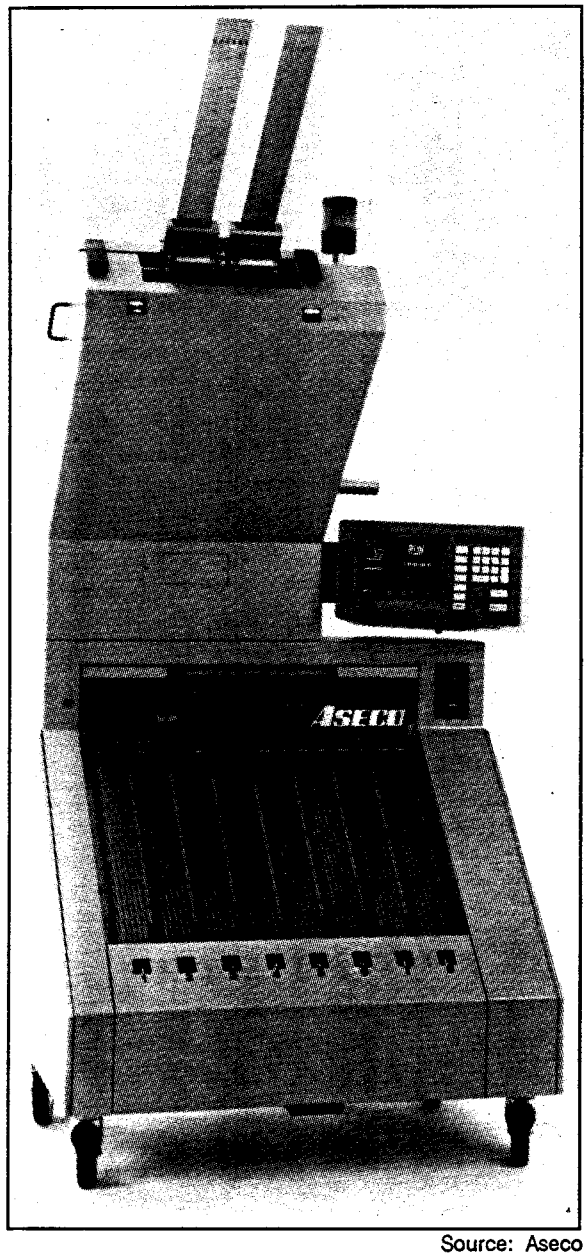
Source: Trigon
2234-83

Presentation 3.4.1.2.1-5

A Trigon bench top handler with dual tube swivel-input and 3-tube output binning.

This latter system is a modernday SOIC handler from ASECO. Note that it has two inputs, each of which will handle two magazines, each with six shipping tubes. The output contains eight magazines. The system also has a hot/cold chamber which will soak the DUT at temperatures between -55 °C and +150 °C.

For temperature control, the hot/cold soak chamber will also contain a conveyor along which the DUT moves. In this case however, it will move along a meandering or spiraling track so that many devices can be kept inside the chamber and soaked for as long a period of time as is necessary to ensure that the DUT has stabilized at the set temperature. Most suppliers provide soak chambers with stabilization times of between 10 and 15 minutes. At 7,000 UPH

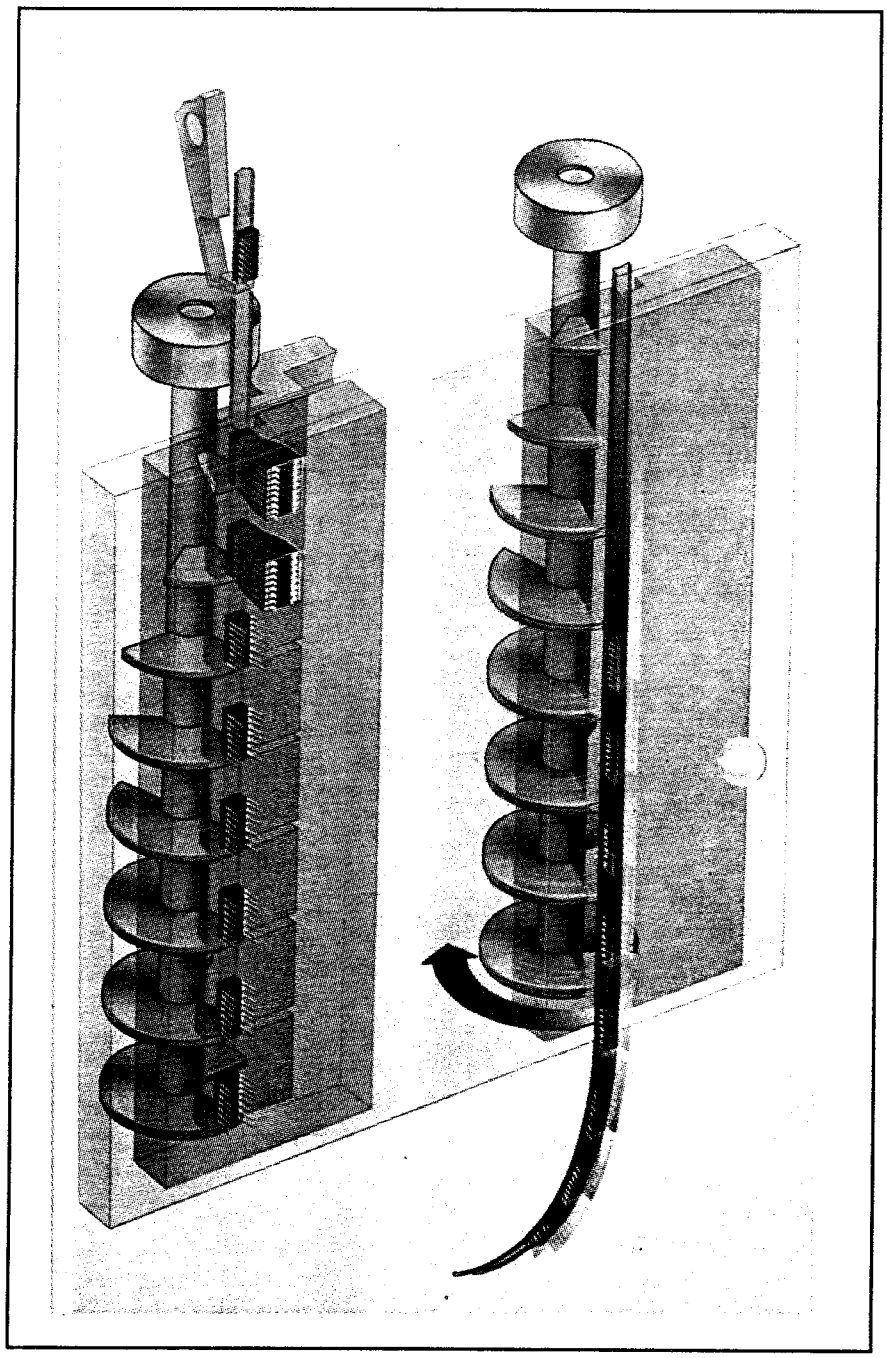


Source: Aseco
2234-84

Presentation 3.4.1.2.1-6

The Aseco S-170 with volume SOIC handler.

throughput, the soak chambers must be capable of holding around 1,500 devices if test throughput is not to suffer. Presentation 3.4.1.2.1-7 depicts the spiral turntable within the Sym-Tek series MTS handler.



Source: Sym-Tek
2234-86

Presentation 3.4.1.2.1-7

Spiral turntable within the soak chamber of a Sym-Tek Model MTS series handler

3.4.1.2.2 Application Technology of Package Handling Equipment

Handler applications invariably begin with emphasis upon the type of package and the number of pins associated with that package. This is because the handler's guide railing and its contactor must be custom fitted to the specific package type, the body width of that package, and sometimes even to the pin count.

Most handler systems are delivered to a customer who will ordinarily use it for just one of two purposes. The first is for those very high volume applications in which the handler can be expected to be used with only one type of package for a long period of time, possibly even for the handler's entire life. The second application is for those low-to-mid-volume applications wherein the contactor is changed frequently to fit varying package types.

More than thirty-five different package types are in use, with pin counts ranging from three pins to more than 524 pins, and body styles that range from thin-body DIP (dual in-line package) to thick body DIPs to square surface mounted packages and many others.

One of the oldest package types is the TO series type, formerly known as a top hat package because it resembles a top hat. These packages were used initially to house transistors. They had three pins. Early integrated circuits also made use of them, so the TO eventually accommodated up to twelve pins. But the pins were long and axial and tended to entangle themselves with the pins from other TO packages. The advent of the short-pinned DIP in the sixties provided a universal package which permitted both high volume and high frequency operation in a reliable package.

The venerable DIP lasted to well into the eighties before it began to be displaced by other packages. However, when IC pin count requirements came to range above 64 pins, the excess lead length needed inside the DIP package limited bandpass. Additionally, the excessive size of the DIP took up far too much board space. This was ironic since the introduction of the DIP was first brought about in order to save board space.

Still, the DIP constituted the largest proportion of packages, even into the nineties. Presentation 3.4.1.2.2-1 depicts the approximate worldwide consumption of packages for 1990 by both package type and by pin count. Note that DIP and TO package styles still prevail. More recent data can be found in Section 1.9.2.

At pin counts above 40, surface mount devices finally displace DIPs, however the overall usage is still small. Nevertheless, pin counts have risen and it can be expected that still higher pin count devices will be needed. New package styles are evolving to accommodate these needs. Presentation 3.4.1.2.2-2 helps outline this direction. It depicts the packaging roadmap envisioned by Texas Instruments.

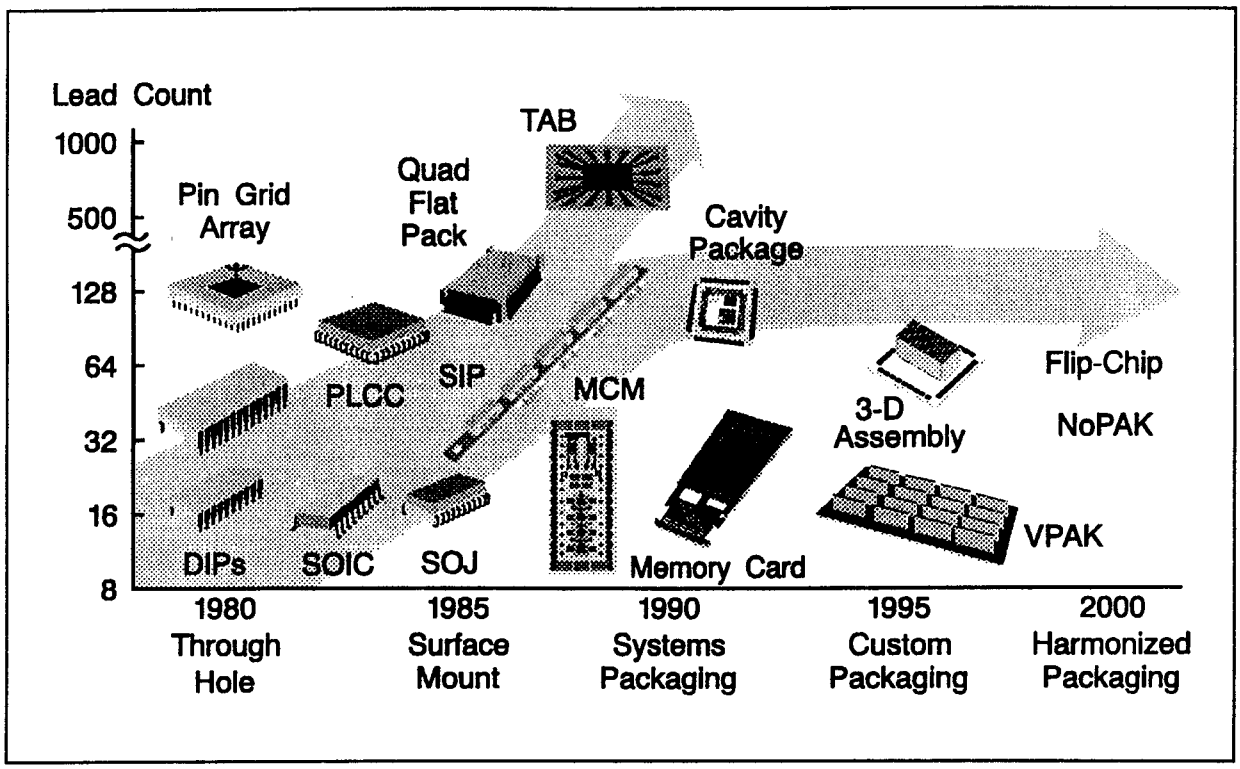
The principal packaging types to displace DIPs in the eighties were PLCCs, pin grid arrays and quad flat packs. SOIC and SOJ (small outline packages) evolved to permit higher packing densities but retained small pin counts. Pin grid arrays were at first thought to be able to handle very large pin counts but it was soon found that they could not. Pin grid arrays tend to peak out in the 200 to 300 pin range; somewhat higher than PLCCs but not as great as TAB. Tab seems to be the only technology capable of penetrating into the 500, or greater, pin count range. Such ranges will be needed eventually for ULSI, as can be again noted from Rent's rule. Rents's rule states that pin count in digital devices will generally vary as the square root of the number of gates. Consequently, a 500 pin package will carry

WORLDWIDE PACKAGE DEMAND BY PACKAGE TYPE

(in millions of units for 1990)

		Lead Count									
		2-4	5-6	7-10	11-16	17-24	25-40	41-64	65-96	97-256	>256
DISCRETE & POWER	101381.1	99908.9	1403.2	45.1	23.9	0.0	0.0	0.0	0.0	0.0	0.0
SOT	10693.3	10693.3	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
Other TO	90687.8	89215.6	1403.2	45.1	23.9	0.0	0.0	0.0	0.0	0.0	0.0
INTEGRATED CIRCUITS	53676.5	0.0	115.7	3280.6	25361.3	10699.2	6455.7	2644.7	3138.6	1682.3	298.4
Through Hold Mount	32218.9	0.0	98.3	2240.7	21341.0	6307.7	1986.6	54.0	109.4	68.6	12.5
SIP & ZigZag	2775.6	0.0	98.3	1336.0	1237.0	74.8	22.1	7.4	0.0	0.0	0.0
Plastic DIP	27661.8	0.0	0.0	890.0	18735.9	6128.4	1907.5	0.0	0.0	0.0	0.0
PPGA	42.6	0.0	0.0	0.0	0.0	0.0	0.0	0.0	24.3	12.8	5.6
CPGA	160.5	0.0	0.0	0.0	0.0	0.0	5.3	7.3	85.2	55.8	6.9
CERDIP	1422.7	0.0	0.0	12.4	1299.1	84.7	23.6	2.9	0.0	0.0	0.0
Multilayer Ceramic DIP	155.6	0.0	0.0	2.3	68.9	19.8	28.2	36.4	0.0	0.0	0.0
Surface Mount	18255.5	0.0	17.4	1039.9	2688.1	3344.6	4201.7	2484.0	2677.2	1516.9	285.9
Chip Carriers	8453.5	0.0	0.0	0.0	0.0	1454.8	1602.0	916.8	2677.2	1516.9	285.9
PLCC	3491.9	0.0	0.0	0.0	0.0	1454.8	1228.6	340.8	194.1	273.6	0.0
Quad Flat Pack	4946.1	0.0	0.0	0.0	0.0	0.0	366.1	571.1	2481.4	1241.6	285.9
Molded Carrier Ring	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CLCC	5.1	0.0	0.0	0.0	0.0	0.0	0.0	2.1	1.3	1.7	0.0
Ceramic Flat Pack	10.5	0.0	0.0	0.0	0.0	0.0	7.3	2.8	0.4	0.0	0.0
Small Outline	9802.0	0.0	17.4	1039.9	2688.1	1889.8	2599.6	1567.2	0.0	0.0	0.0
SOIC Narrow Body	3739.7	0.0	17.4	1039.9	2682.4	0.0	0.0	0.0	0.0	0.0	0.0
SOIC Wide Body	5380.0	0.0	0.0	0.0	5.7	1207.9	2599.2	1567.2	0.0	0.0	0.0
TSOP & STSOP	0.4	0.0	0.0	0.0	0.0	0.0	0.4	0.0	0.0	0.0	0.0
SOJ	677.7	0.0	0.0	0.0	0.0	677.7	0.0	0.0	0.0	0.0	0.0
Ceramic SO	4.2	0.0	0.0	0.0	0.0	4.2	0.0	0.0	0.0	0.0	0.0
Multi-Chip Modules	3202.0	0.0	0.0	0.0	1332.2	1047.0	267.4	106.7	352.0	96.8	0.0
Smart Card	54.2	0.0	0.0	0.0	0.0	20.1	34.0	0.0	0.0	0.0	0.0
MCM-Laminate	2496.7	0.0	0.0	0.0	1332.2	1011.5	153.0	0.0	0.0	0.0	0.0
MCM-Ceramic	649.8	0.0	0.0	0.0	0.0	15.3	80.4	106.7	352.0	95.4	0.0
MCM-Plastic	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
MCM-Exotic	1.4	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	1.4	0.0
TOTAL	155057.5	99908.9	1518.9	3325.7	25385.2	10699.2	6455.7	2644.7	3138.6	1682.3	298.4

Source: VLSI RESEARCH INC
2234-87L



Source: Texas Instruments
2234-89

Presentation 3.4.1.2.2-2

TI's packaging roadmap.

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the industry well into the sea-of-gates region exceeding 300,000 gates. Pin grid arrays tend to peak out at about 300 to 325 pins, or roughly 100,000 gates.

The down side of the packaging issue, as can be seen from Presentation 3.4.1.2.2-1 is that by-far-the-largest-quantity of devices are made with fewer pins, but in numerous packaging styles. This produces severe pressures on handler suppliers to develop adaptable contactors and railings that can handle these numerous configurations. The pressure will not likely abate, for most suppliers now routinely handle most every package style available in order to address their own customers needs. The next three tables show the extent of packaging styles available from TI, National Semiconductor and LSI Logic (see Presentation 3.4.1.2.2-3, 4&5).

As packages become more complex, lead pitch eventually comes to dominate. This can be seen by reviewing these three presentations. The older packages, such as DIPS, are dominantly supplied with a 100 mil pitch. A 100 mil pitch is, of course, a symmetrical spacing of 20 to 25 milliinch wide pins, each separated by 75 to 80 mil spacings on a 100 mil center. Consequently, only 10 pins can be placed in a one inch distance. A 64 pin DIP has 32 pins per side and is, of necessity, 3.2 inches long from pin-end-to-pin-end. The actual package length is slightly longer, typically 3.25 inches.

Texas Instruments

Presentation 3.4.1.2.2-3

Packages available from Texas Instruments

	LEAD COUNT (QTY)									LEAD PITCH (mil)				
	≤16	≤24	≤40	≤68	≤124	≤150	≤196	≤244	>244	100	50	25	20	10
Through Hole Mount														
TO SERIES	3_p—12_p													
MOLDED DIP	8_p			68_p						p				
SWB DIP														
CERDIP														
CERAMIC DIP	8_p			64_p										
SIP			32_d	44_d						p				
ZIP	16_s—20_s									p				
QUIP														
PPGA						145_p				p				
CPGA				68_p				244_p	350_d	p				
Surface Mount														
SOIC Narrow	8_p—16_p										p			
SOIC Wide	16_p			68_d							p	d		
SOIC (Other Width)	16_p—28_p		d	d							d			
SO-J (.300)		20_p									p			
SO-J (Other Width)														
LCCC		18_p		68_p	84_s							p		
LPCC														
PLCC														
J-Lead		20_p			84_p						p			
Gull-Lead														
Butt-Lead														
C-Lead														
CLCC														
Ceramic Flat Pak														
J-Lead														
Gull-Lead														
Butt-Lead														
C-Lead														
QFP (Quad Flat Pack)			40_d					244_d				d		
QFP with Bumpers					124_p		196_p						p	
TAB	8_d							244_d						
COB	16_d									d				
Butt Lead CC														
Specials														
Multi-chip chip carrier			44_d	64_d							d			
SSOP	8_p			56_p								p		

Source: VLSI RESEARCH INC

National Semiconductor Corp.

Presentation 3.4.1.2.2-4

Packages available from National Semiconductor

	LEAD COUNT (QTY)									LEAD PITCH (mil)				
	≤16	≤24	≤40	≤68	≤124	≤150	≤196	≤244	>244	100	50	25	20	10
Through Hole Mount														
TO SERIES	2_p–10_p									p				
MOLDED DIP	14_p			64_p						p				
SWB DIP	14_p		48_p							p				
CERDIP														
CERAMIC DIP	8_p			64_p						p				
SIP	11_p									p				
ZIP														
QUIP														
PPGA				68_p					323_p	p				
CPGA		28_p							323_p	p				
Surface Mount														
SOIC Narrow	3_p–16_p										p			
SOIC Wide	10_p–28_p										p			
SOIC (Other Width)														
SO-J (.300)														
SO-J (Other Width)														
LCCC		18_p			124_p						p			
LPCC														
PLCC														
J-Lead		20_p			124_p						p			
Gull-Lead														
Butt-Lead														
C-Lead														
CLCC														
Ceramic Flat Pak			44_p		124_p						p			
J-Lead														
Gull-Lead														
Butt-Lead														
C-Lead														
QFP (Quad Flat Pack)					100_p				256_p		p	p	p	
QFP with Bumpers														
TAB														
COB														
Butt Lead CC														
Specials														
_____														
_____														
_____														

Source: VLSI RESEARCH INC

LSI Logic Corp.

Presentation 3.4.1.2.2-5

Packages available from LSI Logic

	LEAD COUNT (QTY)									LEAD PITCH (mil)				
	≤16	≤24	≤40	≤68	≤124	≤150	≤196	≤244	>244	100	50	25	20	10
Through Hole Mount														
TO SERIES	.	.	.	.	.	.	.	.	.	.	.	.	.	.
MOLDED DIP	14_p	——	——	48_p	.	.	.	.	.	*p*	.	.	.	.
SWB DIP	.	.	.	.	.	.	.	.	.	.	.	.	.	.
CERDIP	.	.	.	.	.	.	.	.	.	.	.	.	.	.
CERAMIC DIP	14_p	——	——	64_p	.	.	.	.	.	*p*	.	.	.	.
SIP	.	.	.	.	.	.	.	.	.	.	.	.	.	.
ZIP	.	.	.	.	.	.	.	.	.	.	.	.	.	.
QUIP	.	.	.	.	.	.	.	.	.	.	.	.	.	.
PPGA	.	.	.	68_p	——	——	180_p	.	.	*p*	.	.	.	.
CPGA	.	.	.	64_p	——	——	——	——	391_p	*p*	.	.	.	.
Surface Mount														
SOIC Narrow	.	.	.	.	.	.	.	.	.	.	.	.	.	.
SOIC Wide	.	.	.	.	.	.	.	.	.	.	.	.	.	.
SOIC (Other Width)	.	.	.	.	.	.	.	.	.	.	.	.	.	.
SO-J (.300)	.	.	.	.	.	.	.	.	.	.	.	.	.	.
SO-J (Other Width)	.	.	.	.	.	.	.	.	.	.	.	.	.	.
LCCC	.	20_p	——	——	——	148_p	.	.	.	*p*	.	.	.	.
LPCC	.	.	.	.	.	.	.	.	.	.	.	.	.	.
PLCC														
J-Lead	.	.	28_p	——	——	132_p	.	.	.	.	*p*	.	.	.
Gull-Lead	.	.	.	.	.	.	.	.	.	.	.	.	.	.
Butt-Lead	.	.	.	.	.	.	.	.	.	.	.	.	.	.
C-Lead	.	.	.	.	.	.	.	.	.	.	.	.	.	.
CLCC														
Ceramic Flat Pak	.	.	40_p	——	——	——	——	——	300_p	.	*p*	.	.	.
J-Lead	.	.	.	.	.	.	.	.	.	.	.	.	.	.
Gull-Lead	.	.	.	.	.	.	.	.	.	.	.	.	.	.
Butt-Lead	.	.	.	.	.	.	.	.	.	.	.	.	.	.
C-Lead	.	.	.	.	.	.	.	.	.	.	.	.	.	.
QFP (Quad Flat Pack)	.	.	44_p	——	——	160_p	.	.	.	.	.	*p*	.	.
QFP with Bumpers	.	.	.	.	.	.	.	.	.	.	.	.	.	.
TAB	.	.	.	.	.	.	.	.	.	.	.	.	.	.
COB	.	.	.	.	.	.	.	.	.	.	.	.	.	.
Butt Lead CC	.	.	.	.	.	.	.	.	.	.	.	.	.	.
Specials														
TQFP	.	.	.	.	.	164_p	.	.	.	.	.	*p*	.	.
TQFP	.	.	.	.	.	196_p	——	224_p	.	.	.	.	*p*	.
TQFP	.	.	.	.	.	.	.	260_p	—— 524_p	.	.	.	.	*p*

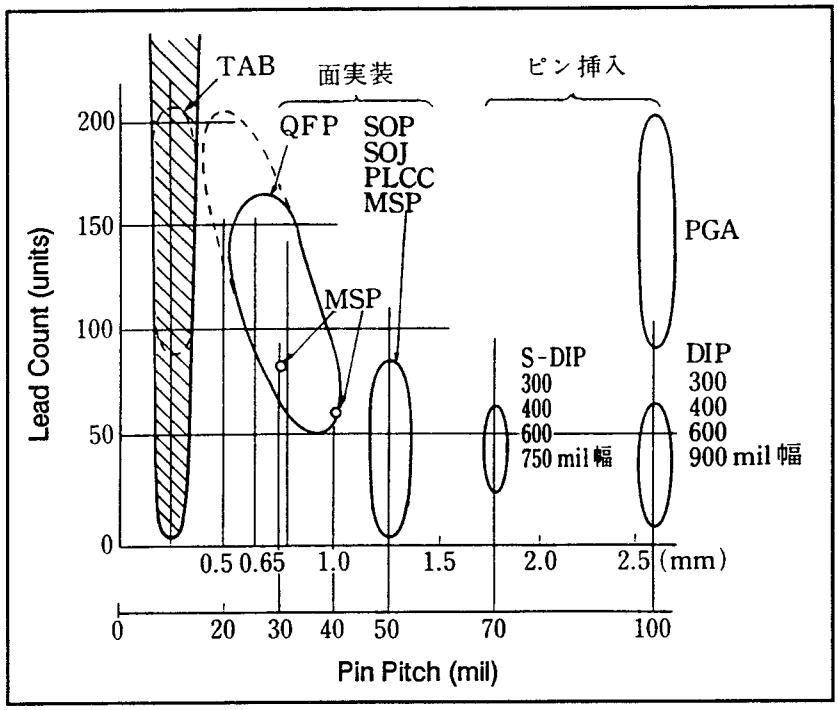
Source: VLSI RESEARCH INC

2234-92W

By halving the pitch, the pin density can be doubled or, alternatively, the package length can be halved. The problem presented is that the contactor metal must now also behalved while maintaining the same approximate lifetime in terms of number of flexures before failure. The data in the three tables indicates that most semiconductor suppliers are being forced to resort to ever smaller pitches, with some now being as low as 20 mils. Tape quad flat packs drop still lower, to 10 mil pitches.

Presentation 3.4.1.2.2-6 depicts a chart from the Japanese textbook 'Emerging TAB Technology' that shows where the Japanese believe lead count and lead pitch is headed. Here it can be noted that Quad flat pack and TAB—namely tape quad flat pack such as produced by LSI Logic—are about the only packages able to simultaneously handle both high pin count and very fine pitch geometries. These are clearly the packages of the future.

As pitch continues to decrease, it eventually reaches the limits of the wire bond itself. This is the limiting factor. Today, most wire bonds are placed on a 6 mil pitch, with a 4 mil pad and a 2 mil spacing. Some wire bonding suppliers say they can go down to a 3 mil pitch, but the cost becomes excessive, as was shown back in Section 3.4.1.1 concerning probers. Under these circumstances, the silicon substrate itself can become the lead frame while the outside wiring connects directly to the pad. This is almost what happens with the SSOP package, but not quite. Still, such small packages seem to be better handled with tape than singly or by shipping tube or carrier. Consequently, it can be expected that tape packs will more and more come to dominate the handler business.



Source: Emerging TAB Technology, 1989
2234-93

Presentation 3.4.1.2.2-6

Lead count versus lead pitch

3.4.1.3 Laser Repair Systems

The laser repair system industry is somewhat monolithic but has three, and possibly four, minor subsegments. The major three are IC trim, IC repair, and hybrid trim. The fourth segment is sometimes called memory repair. However since most IC repair is for memory repair, we include it in the generic category of IC repair. These systems are similar enough that they are discussed as one market, even though market-wise they are carried as three.

Laser repair systems are carried in this section as material handling equipment even though the terminology is not quite correct. This is because they fit into this category better than in any other.

Laser systems, in some ways, have the best of all worlds and the worst of all worlds. They must combine critical aspects of testing, wafer probing and lithography. Consequently, the systems must have extremely high precision as well as high speed. In contrast, the wafer prober only needs to position itself mechanically while the tester only needs to be able to test electrically. In order to be of use, a laser system must be able to place a laser on a conductor that is almost as narrow as the limiting line-width technology allowed by the stepper in use. This is typically 1 to 5 microns with better than 1/2 micron accuracy. Contrast this with a prober placement requirement of 25 to 30 microns with accuracy in the 4 to 5 micron range. Laser systems must also be able to accept a set of defective site patterns from the test equipment and translate these into an actual geometrical layout pattern. It then must find the site. Finally, the system must be able to cut the conductor without causing damage to surrounding material.

The market size for laser repair systems is mid-range. In 1990, it amounted to $98M. More than one dozen suppliers compete in the market. Major suppliers include ESI (Electro Scientific Industries Inc), Nikon, Chicago Laser Systems, Teradyne Laser Systems Inc and XRL.

3.4.1.3.1 Development of the Industry

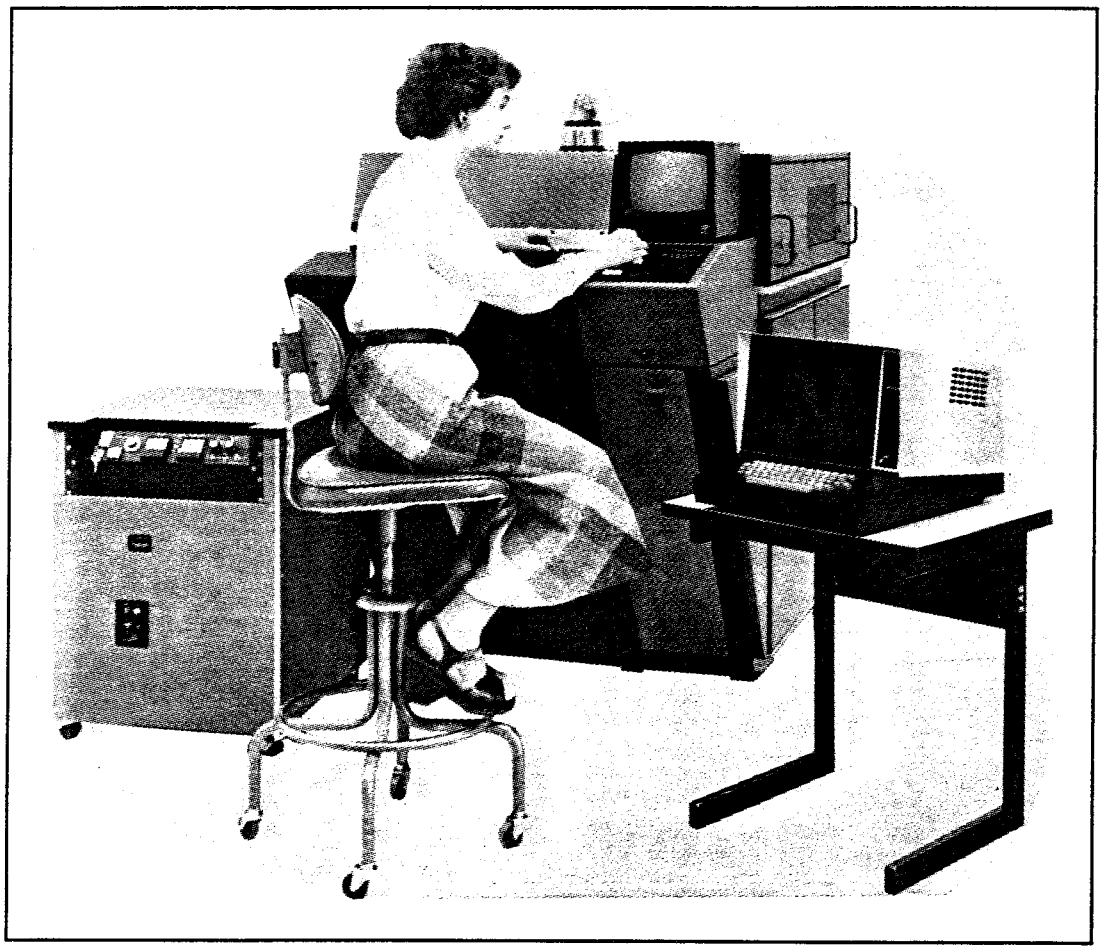
Laser repair is an outgrowth of laser trimming, which came to the forefront in the mid sixties. Linear integrated circuits were just developing. The IC op amp had been invented by Bob Widlar at Fairchild. This was a major industry contribution which literally created an entire new industry segment. To work properly, the op amp needed precision resistors. IC resistors are notoriously variable, sometimes varying by as much as 30%, but needing to be in the 0.1% to 1.0% range. Laser resistor trimming proved to be an ideal way to obtain high precision by trimming the resistor after the circuit was completed. Usually the resistor was initially designed lower in resistance than the targeted value. Then a cut was made in the body of the resistor to increase its resistance. The cut was usually in the shape of an I, an L or a J along the body of the resistor. The changing resistance of the resistor was monitored while the cut was being made so that work could be stopped at the targeted value.

It is not certain which company was actually the first to initiate laser trimming. However, by the late sixties these systems were being used by many companies. It is believed that ESI and Teradyne were the first two companies in the commercial business. Teradyne provided linear testers to the industry. It needed a way to improve testing, consequently it entered the market as a natural extension to its ATE equipment. Chicago Laser Systems entered the market

in the mid-seventies while XRL entered in 1984. In 1989 Teradyne spun-off its laser repair equipment and merged with another small company to form the independent company now named Teradyne Laser Systems Inc. Teradyne Laser Systems Inc is sometimes called TLSI, but should not be confused with the company by the same name on Long Island.

Presentation 3.4.1.3.1-1 depicts an early ESI Model 44 trimming system. This machine was introduced in the seventies. It worked over a 3x3 inch area, barely enough for a three inch wafer, and could trim with kerf widths down to about 10 microns. The system used a DEC PDP-11 computer and a 3 watt Nd:YAG laser. The Model 44 was a venerable system, and after various redesigns survives today as the Model 44 plus, but as a hybrid trimming system, rather than an IC trimming system.

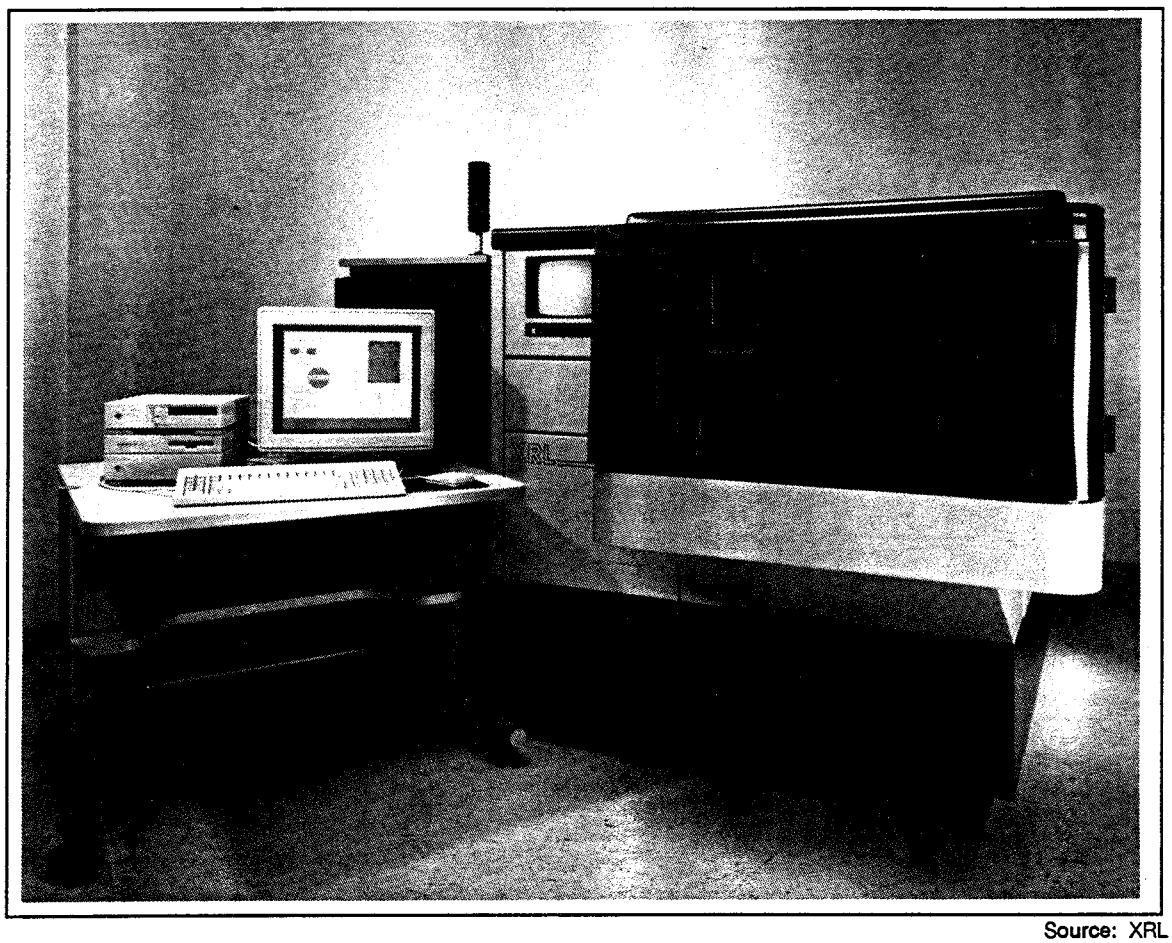
A more modern version of an IC repair system is shown in Presentation 3.4.1.3.1-2. This is the XRL model 1025. It was introduced in mid 1990. Functionally, it is the same as the earlier version of the ESI



Source: ESI
2234-94

Presentation 3.4.1.3.1-1

The ESI Model 44 laser trimming system.



Source: XRL
2234-119

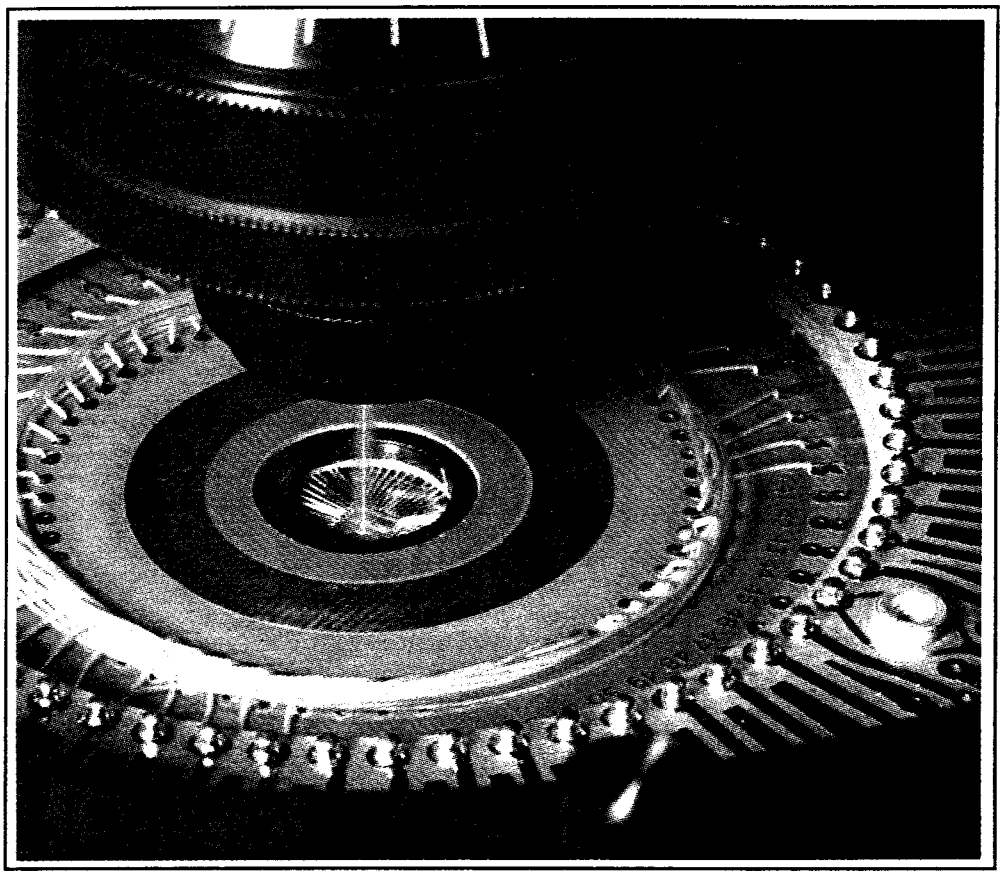
Presentation 3.4.1.3.1-2

The XRL Model 1025 laser repair system.

model, however it has much greater precision for use with modern IC memories, is totally automated, and is clean room compatible.

3.4.1.3.2 Application Technology

As mentioned previously, a laser repair system consists of a fine-positioning X/Y table that can place an IC accurately under an optical table. Having done this, a fine laser beam is directed onto the wafer to cut a wire. Presentation 3.4.1.3.2-1 depicts a typical system at work. Here, it can be seen that the system consists of an elaborate prober with probe card and electrical contacts to turn-on the device. The laser beam can be seen coming down through the lens onto the wafer. A more global overview can



Source: ESI
2234-96

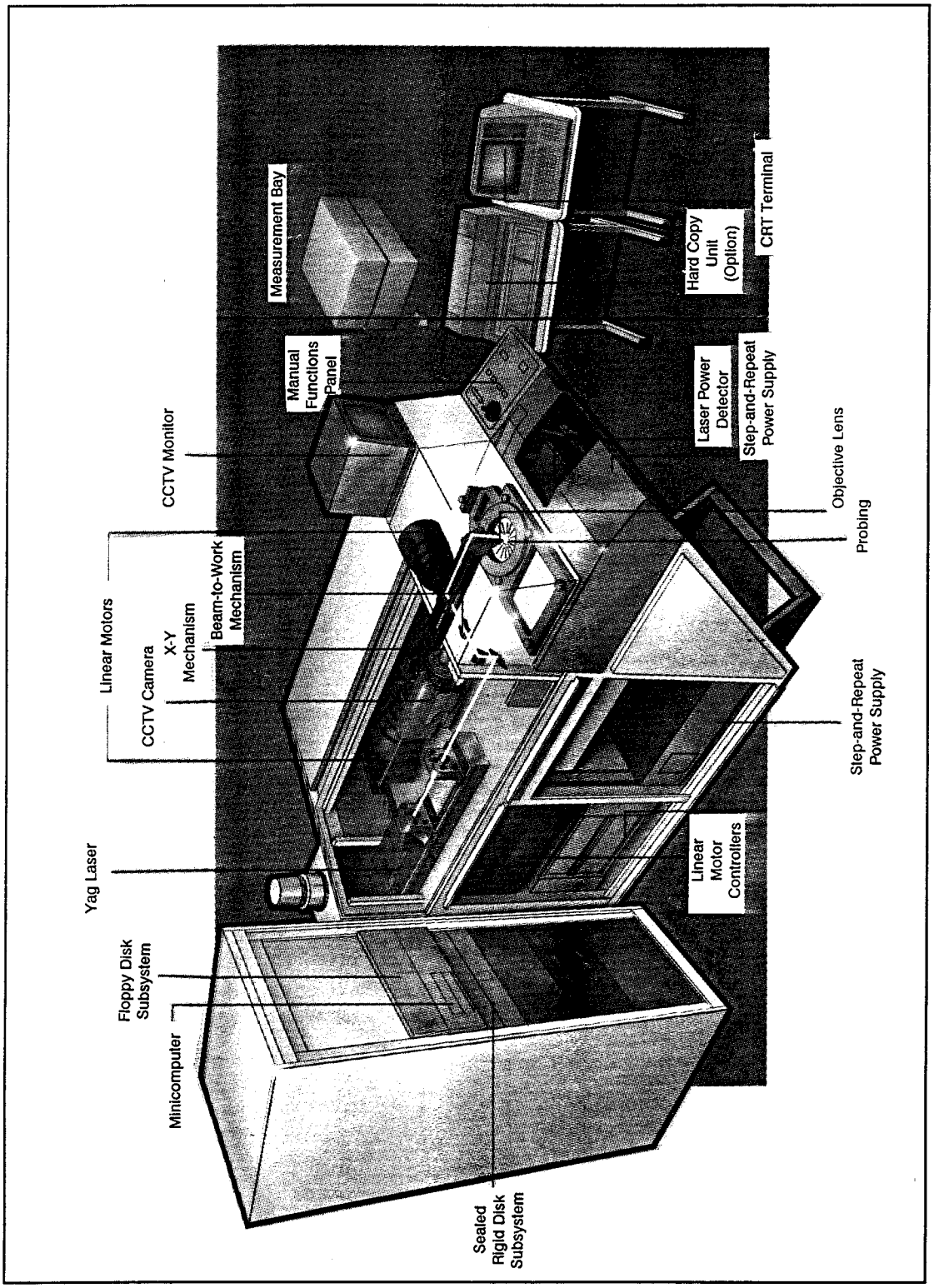
Presentation 3.4.1.3.2-1

The ESI Model 8000 at work.

be seen from the next Presentation 3.4.1.-3.2-2. Here, the entire system concept can be seen.

The chief differences in the various types of machines are in speed of operation, application, laser source in use and laser deflection method. Hybrid systems typically must cut larger conductors so they have beam spot sizes of about 25 to 30 microns. IC systems typically have spot sizes of about 2.5 to 3.0 microns if they use Nd:Yag or Nd:YLF lasers.

TLSI, Chicago Laser and XRL use a galvanometer to deflect the laser while ESI uses a recoilless linear drive motor. The galvanometer consists of a mirror mounted onto a galvanometer coil instead of a meter pointer. The mirror is rotated by use of an electrical current. The laser beam directed at and reflected from the mirror is deflected



Source: ESI 2234-97

Presentation 3.4.1.3.2-2

System configuration of the ESI Model 80.

from its nominal path in proportion to the angle that the mirror is deflected by the current through the galvanometer. In the ESI method, the laser is directed perpendicularly to the work piece at a fixed point in the XY plane of the work-piece surface. The beam deflecting mechanism is mounted on the recoilless linear drive motor.

There are pro and con arguments about both approaches. Some users prefer one while some prefer the other. Both methods give comparable minimum spot size, work-piece field size, accuracy and resolution. Typical specifications for four modern systems are shown in Presentation 3.4.1.3.2-3 below. All can be seen to be comparable in minimum spot size. The XRL is superior in system accuracy.

The XRL deserves special mention in speed. It is the newest system. As such it was designed with ASIC applications in mind. The repair of memories might need 20 to 50 links blown altogether while ASICs might need several thousand. So, the XRL system uses a raster-scanning-beam that can operate on-the-fly where speed, rather than accuracy, is critical. It also uses the slower random-access method as well.

Presentation 3.4.1.3.2-3

Typical Specifications

		ESI L9000	*XRL* 1025	*TLSI* M228	*Nikon* LR-2F
Laser type		Nd:YLF	Nd:YLF	Nd:YLF	Nd:YLF
Wavelength	(nM)	1047	1047	1047	1047
Minimum spot size	(μ)	2.5	2.5	2.8	2.5
Maximum spot size	(μ)	13.0	6.0	4.5	10.0
Field size	(mm x mm)	35 x 35	26 x 26	20 x 20	
System resolution	(μ)	±0.08	±0.0015	±0.08	±0.05
System accuracy	(μ)	±0.5	±0.35	±0.5	±0.5
Random access repair speed	(links/sec)		100-200		
Raster scan repair speed	(links/sec)		2000		
Wafer setup time	(seconds/8" wafer)	<5	<12		
Field-to-field positioning time	(sec/field)				~0.150
Field alignment time	(sec/field)				
Auto focus time	(sec/field)				
Throughput @ 25 links/die @ 8 memory die/field	(die/hour)			>1800	

Source: VLSI RESEARCH INC

2234-120W