3.3 AUTOMATIC TEST SYSTEMS

3.3 Automatic Test Systems

- **ATS is segmented into three sub-markets: Component test, burn-in and design diagnostics.**
- **Component test includes three sub-markets: Logic, memory and linear.**
- **Burn-in includes three sub-markets: Monitored, dynamic and static.**
- **Design diagnostics includes circuit probers and modification tools.**

Automatic Test Systems (ATS) encompass a broad range of equipment—in size and in function as well as in price. It includes all equipment that is used to electrically verify a device's functionality. VLSI Research has adopted the automatic test systems flow chart listed in Figure 3.3.0.0-1. The categorization of test systems is further subsegmented in order to more appropriately group comparable test equipment. For example, logic testers are grouped into eight classes. These range from class 0 through class seven. The higher class numbers denote more complex systems.

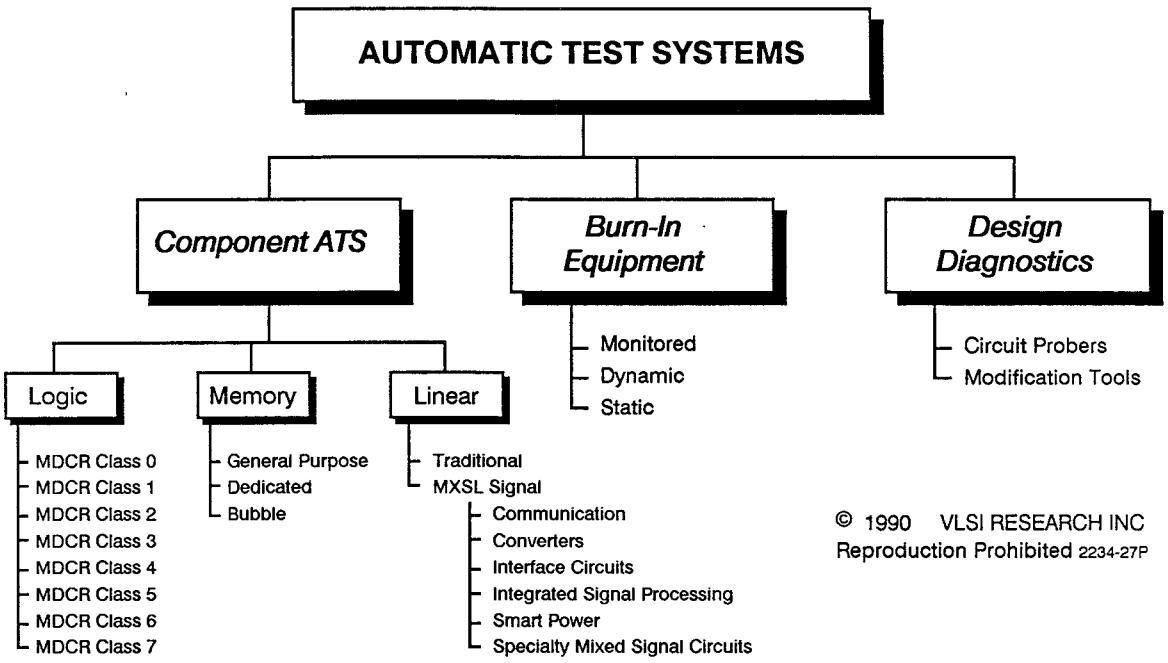
Linear testers likewise are categorized into two groups—those test systems which perform the more traditional linear tests, and those which perform 'mixed signal' testing. Consequently, linear test systems are designated as either *traditional or mixed signal.* The mixed signal test systems are further segmented based on the primary application of the mixed signal test system.

Burn-In is segmented into three types of equipment: Monitored, dynamic and static. These segments encompass equipment used for quality control that is indigenous to semiconductor manufacturing.

Design Diagnostics includes equipment used during the design phase to verify, or to modify a device to achieve some predetermined functional behavior so it can be manufactured in volume. This includes in-circuit probers such as E-beam or laser beam probers and modification tools such as Focus Ion Beam Systems.

In general, testing—as it occurs within a semiconductor manufacturing facility—is an extension of the quality control department. Its roots go back to the earliest concepts of inspection for form, fit and function. Early in the life of the semiconductor industry, however, testing split away from quality control to become an entity in its own right. The concepts of testing encompass two key areas within a manufacturing environment. The first is wafer probe. The second is final test.

Figure 3.3.0.0-1



Historically, every semiconductor device manufactured has been tested. While there are some factories that have sample test, this has been a rare occurrence. When sampling test methods are used, there is little economic pressure to stress how quickly the test must be made. However, when more testing is required, speed is a primary concern because it determines the throughput and economics of the factory. Consequently, in those areas where more testing is performed, automated handling and testing equipment have come more into play.

In general, a device will be tested at several different points during the manufacturing process. These points are shown in Figure 3.3.0.0-2 which illustrates an abbreviated flow chart that traces manufacturing from wafer probing through shipment. Devices receive their first electrical test as a completed unit while still in die form at wafer probe. Manufacturers call this die sort, electrical sort or wafer sort.

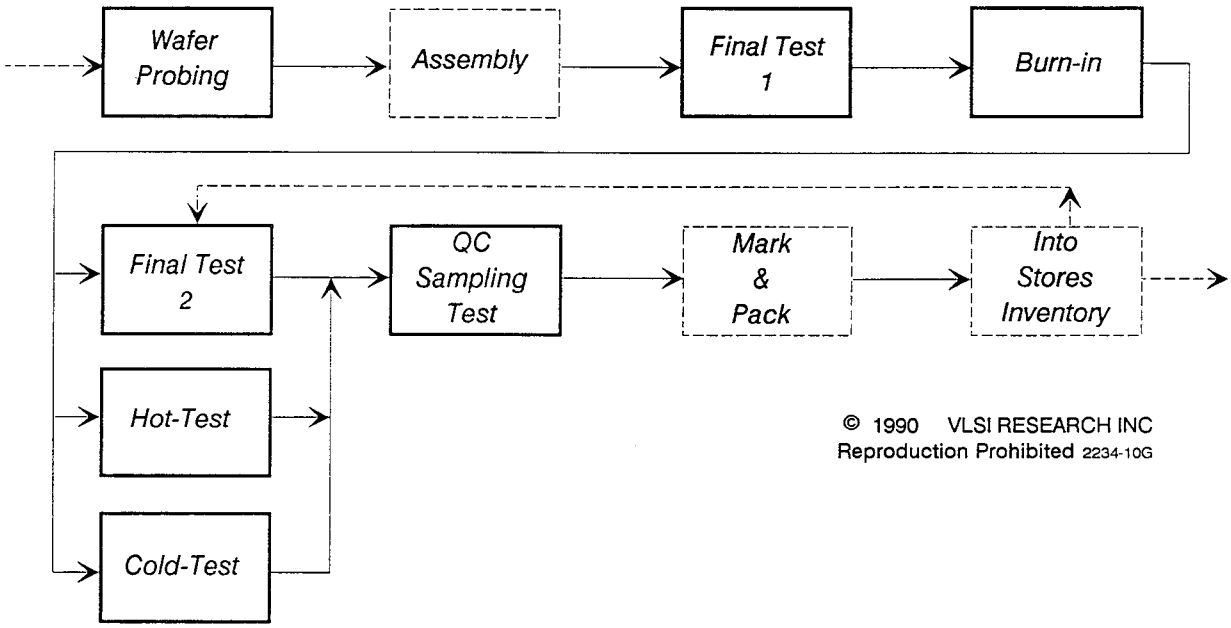
This electrical test signifies testing of each die on a wafer via automated electrical test equipment, or 'Automatic Test Systems' as they have come to be called.

Devices will receive their first test in packaged form at 'final test'. Final test normally consists of a three part test. These include testing at ambient (room) temperature, testing at the device's upper temperature limit and testing at its lower temperature limit. Environmental and sample electrical tests will be conducted later.

Sometimes, parts are pulled from inventory and regraded. This occurs, for example, if

Figure 3.3.0.0-2

TEST POINTS IN SEMICONDUCTOR MANUFACTURING



a 'B' grade unit is needed but only 'A' grade parts are available, or if a customer orders specialized testing. On these occasions, material may be returned to have additional testing performed.

Consequently, in the flow of testing, some devices may be tested several times while others might be tested just a few times. In fact, some devices could be tested as many as five times if they received both a pre-burn-in and a post burn-in test, a QC test, and are then recycled from stores for re-grading. On average, each device will be tested 2.5 times as it is produced. Once at wafer probe, once at final test and an additional one-half time or so when averaged across all other test points.

3.3.1 CURRENT INDUSTRY CHARACTERISTICS OF ATS

(Index continued on next page)

3.3.1 CURRENT INDUSTRY CHARACTERISTICS OF ATS

(Index Continues)

3.3.1 Current ATS Industry Characteristics

- **The semiconductor automatic test system industry arose from in-house design groups.**
- **The founding of Teradyne in 1960 marks the inception of the ATS industry.**
- **Test productivity is a key factor in determining the competitiveness of a semiconductor manufacturer.**

Automatic Test Systems (ATS) exist to ensure the integrity, quality and—to some degree—the reliability of semiconductor components. These testers consist of electronic systems whose function is to generate a large ensemble of signals, to establish the appropriate test patterns, to properly set them in sequence and then use them to drive the semiconductor component itself.

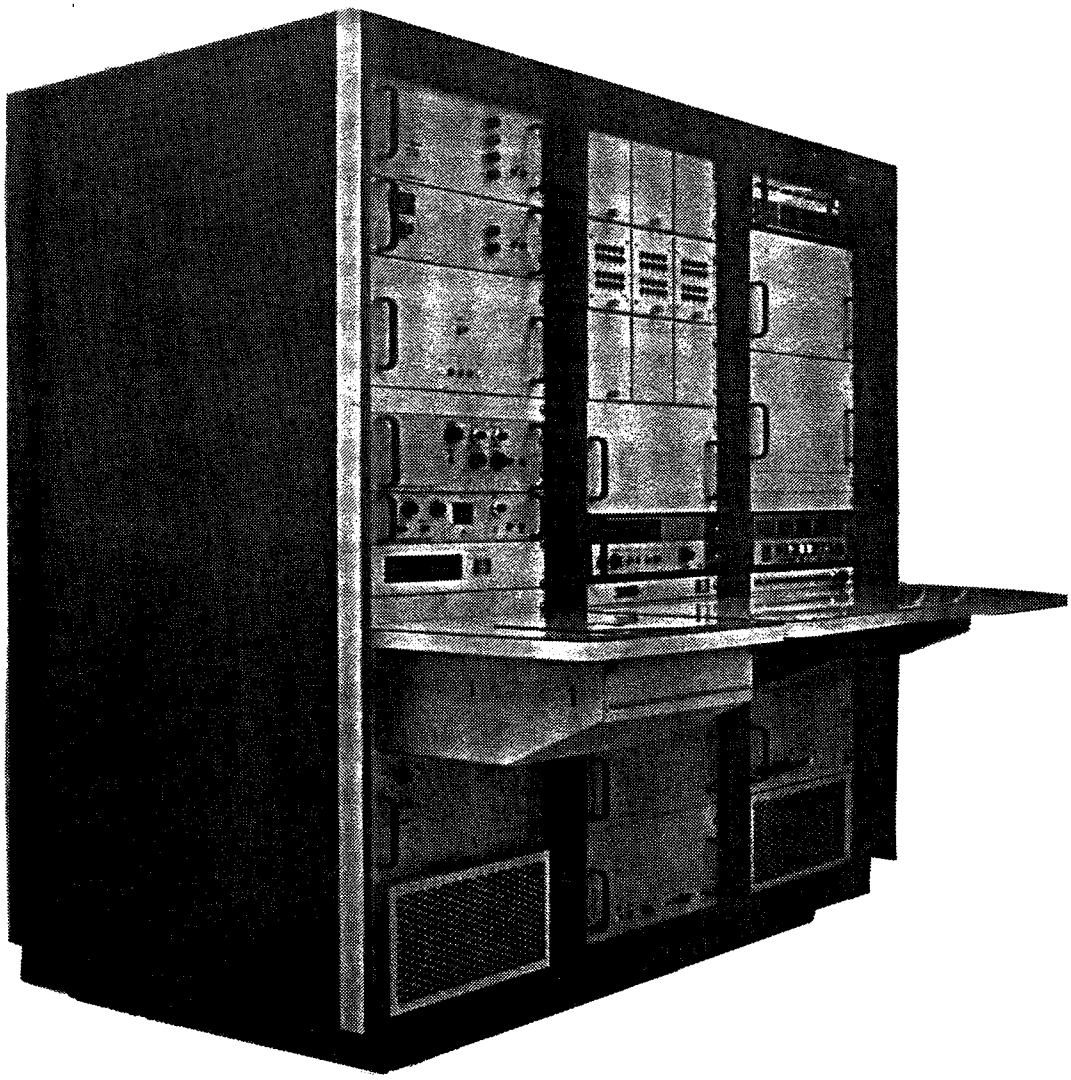
This is all done while the tester is simultaneously establishing an equally large ensemble of expected results with which to compare the component's response. Since these ensembles can often times consist of billions of bits of data, the test system must be quite complex in order to keep everything in place and quite fast in order to get everything done economically and on time. In fact, the technology used is so advanced that semiconductor companies often look to the needs of ATS as key drivers of IC technology.

3.3.1.1 Development of the ATS Industry

Automatic Test Systems had their beginnings in three industries—semiconductors, computers and test & measuring instruments. Vestiges of these industries remain today, but in differing proportions to the impact they have made. It is tempting, but erroneous, to equate Automatic Test systems with the test and measuring equipment industry.

The design of semiconductor test systems arose predominantly from the efforts of in-house design groups at companies such as Fairchild, Signetics and Texas Instruments. Fairchild's earliest full-sized system, the Fairchild 4000 is shown in Figure 3.3.1.1-1. The Signetics test equipment referred to is no longer on the market. At one time this unit was offered as the Signetics Model 1420. Similarly, Texas Instruments at one time offered several testers to the industry. They are now a captive producer of test equipment.

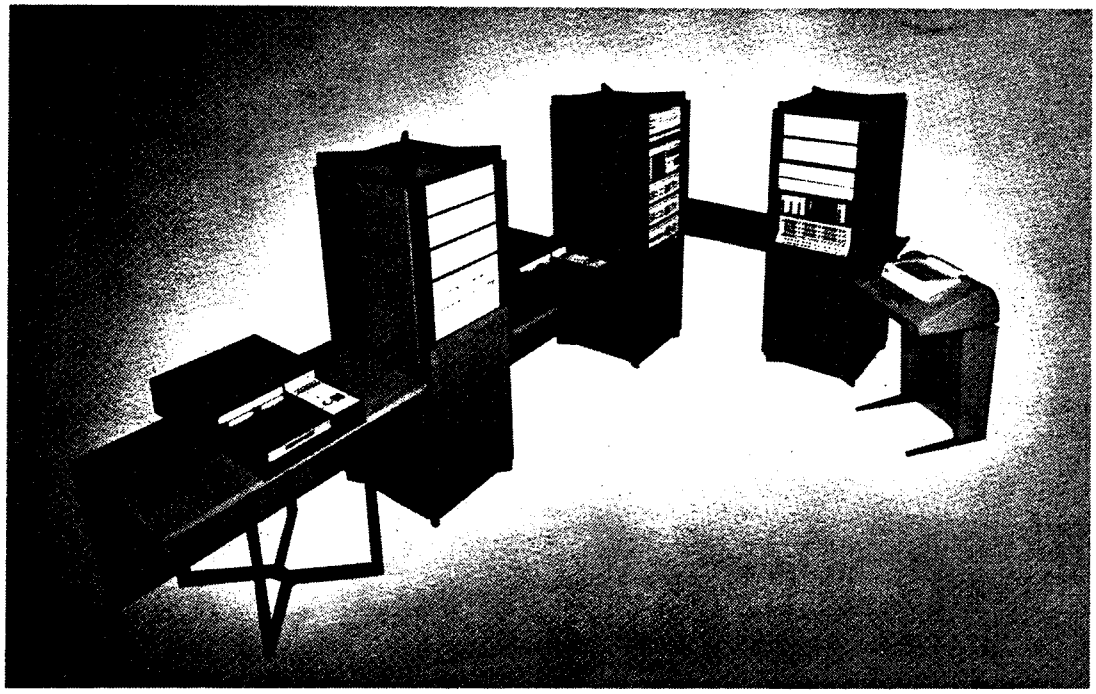
These early companies primarily manufactured test equipment for their own internal use. Teradyne entered the market in 1960 as the very first full-merchant supplier of test equipment. Its first product was a diode tester. The company's first integrated circuit tester, Model J259, was introduced in the mid sixties. This model was soon followed by the J283 'slot' machine (Figure 3.3.1.1-2). A conceptual feeling of the complexity of this era can be appreciated



Ref: Fairchild
2234-13

Figure 3.3.1.1-1

Fairchild Model 4000M System with Model 5800 Dynamic Test Bay



Ref: Teradyne
2234-14

Figure 3.3.1.1-2

The Teradyne J283 SLOT Machine

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from excerpts from the Teradyne J283 brochure:

> The J283 (also called the SLOT Machine because of its Sequential Logic Testing capability) is a high-speed functional and DC parametric test system for digital ICs. Capable of supporting up to eight test stations (manual, automatic, prober, or any combination thereof), it is ideal for any application demanding high productivity.

The J283 is available in configurations with 18, 24, 36, 48, and 60 channels, with possible expansion to 120 channels. The computer is an 18-bit Teradyne M365, and a CartriFile magnetic tape unit is included as standard equipment. Among the many convenient features included is a CRT presentation of the logic applied to any six channels through any 16 steps in the test sequence, an invaluable aid in program debugging.

Features:

- All channels include both drivers and detectors, all under program control.
- Up to eight multiplexed test stations with a single system.
- On-line pattern generation for LSI testing.
- Bipolar and MOS voltage levels.
- Fast, convenient data logging on magnetic tape.
- Interfaces available to all popular handlers and probers.
- Fast (100 kHz) functional testing plus highly precise (1 mV, 1 nA resolution) dc measurements.
- On-line editing, distribution analysis included in Teradyne software.

While this description is archaic by today's test standard, it was very advanced for its time. To see just how advanced, review Jim Healy's description from his book.†

> "Semiconductor ATS had its beginning, as one might expect, in the same place that semiconductors were first produced in quantity. Fairchild Semiconductor recognized the need to automate the test process. Tests on transistors were performed with a separate bench set-up of instrumentation for each type of test. This was a long and laborious process. Each test required that the device be inserted into a different test set-up. It was soon realized that if the device could be tested with a single insertion, the cost of testing could be reduced—to say nothing of the other obvious benefits.
>
> Fairchild's first automatic tester, the Model 300, was built by the newly formed Instrumentation Division. It consisted of a set of different force and measuring units that were constant voltage and current sources. Plug-in cards were used to connect the various instrumentation to the relevant device-under-test terminals. An automatic sequencer selected the proper plug-in cards in the sequence in which they were inserted into the tester. All programming was done by resistor selection on the plug-in cards. To make effective use of the Model 300, the engineer literally had to make resistors. A plug board was used for direct classification of the devices into various pass and fail bins, depending on the test result.
>
> Although primitive, this system worked. That was 1960. Not long after, a company was formed in Boston with a charter to develop semiconductor ATS. The company was called Teradyne, and with its inception the ATS industry was born."

Fairchild introduced the Model 4000 in 1964. The Fairchild Sentry 400 was subsequently introduced in 1969. Generations of integrated circuit testing and test methods date back to innovations made by Teradyne and the Fairchild early machines. A birds-eye view of the history of the industry is shown in Figure 3.3.1.1-3. It depicts the evolution of major lines of equipment by the major suppliers. (The time line is distorted to better accommodate the data.)

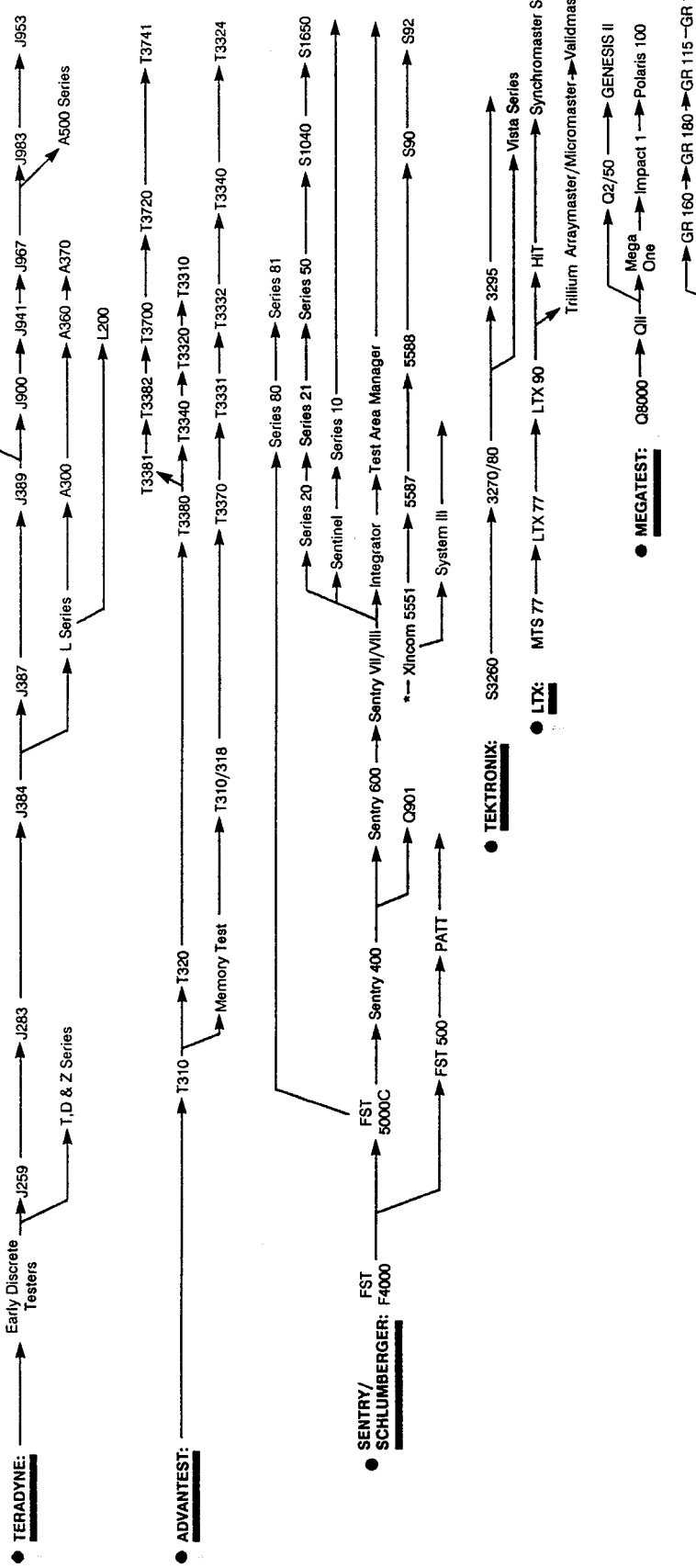
The Impact of End Users

This evolution in test equipment suppliers coincided with changes in the test equipment user's side of the market. In the past, these test equipment users were merely divided into two major segments—the semi-

† James T. Healy, "Automatic Testing and Evaluation of Digital Integrated Circuits", Reston Publishing Co., Inc. 1981.

Figure 3.3.1.1 -3

AUTOMATIC TEST SYSTEM GENEOLOGY



* By Acquisition

conductor producers and the semiconductor users. The former group generated demand for production types of testing while the latter group generated demand for incoming inspection types of testing. Initially, there was approximately a 50-50 split between each segment.

This ratio began to rapidly change in the late seventies. At first, it appeared that much greater activity and interest was being generated in testing for incoming inspection. However, it was soon to become apparent that much of these purchases were for installation in new captive semiconductor manufacturing facilities, rather than at incoming inspection sites. In fact, the equipment was being purchased for use in internal manufacturing purposes and was also being shared with incoming inspection departments for their needs. As time passed, production testing garnered more and more of tester sales. By 1983, production testing accounted for 84% of all test sales while incoming inspection accounted for just 16%. The captive segment accounted for most of this growth. In contrast, in 1977 captive purchases of testers for production amounted to only 12% of the total market.

In addition to the semiconductor industry, the computer industry has had, and continues to have, profound effects upon test equipment. In the early sixties, this was due to the difficulty of testing computers. For example, the uncertain testability of the IBM System 360 and the Illiac IV computer stimulated the development of new test methods by several research teams. These efforts ultimately led to several computer aided test pattern generation methods compatible with computer aided design systems. Roth's 'D' calculus and Seshu's sequential analyzer are two specific methods developed. They created the mathematical framework around which conceptual test systems could be architected. These systems eventually led to the functional testing methods for digital systems. However, VLSI circuits soon became bogged down from the difficult and time consuming methods of functional testing. Once again, the computer industry came to the rescue and solved the problem with on-chip testability methods.

The computer industry's impact on testing is through its customer base rather than through its test groups. It is the availability of inexpensive computers that is allowing the automation of factories. This in turn has caused conventional automatic test equipment to become a part of the control mechanisms used in the automated factory. As the automated factory evolves, it will come to provide the controls necessary to build the part correctly the first time. Hence, 'test' may no longer be needed. This is because 'test' implies that the product might be defective, so it must be completely tested for 'goodness'. However, such an approach has proved too complex and too costly. Since defective devices are caused by process variations, it makes more sense to control the process tightly instead of using the costly approach of testing out process variations on each and every part. Hence, process diagnostics came to be stressed over component testing in the early eighties, resulting in lower ATS market growth.

The computer industry has also had an equally strong role in generating the need for memory test systems, just as it played an important role for other types of test systems, as well as for factory automation. Initial memory efforts were focused on modifying logic testers to test memory devices. This in turn led to separate function generators whose purpose was to produce a defined set of patterns, hence they were first called pattern generators. Today, the pattern generator is a very small part of a memory tester.

Development of Logic Testing

Historically, the emergence of modern ATS was marked by the development of digital test equipment. The digital IC test equipment industry has had the longest and richest history of all. Moreover, it has spawned almost all other test equipment categories. A single exception is the discrete tester segment, which had evolved earlier, and which spawned the digital logic IC test equipment industry.

As mentioned, early developments of digital IC testers included the Fairchild 4000 and the Teradyne J259. By 1970, numerous companies were serving the market. A few notable names included AAI, Birtcher, E-H Research, Fairchild, Macrodata, Hewlett-Packard, Optimized Devices Inc., Signetics, Teradyne, and Texas Instruments. By 1974, just six of these remained.

The industry had its first downturn in 1970, but sales picked up quickly again and several new competitors entered the business. These companies were Ando, Datatron, GenRad, Minato, Takeda Riken—now Advantest, Tektronix and Siemens. Teradyne remained the leader during that period. By August of 1974, Teradyne was reporting quarterly sales of $15.3 million for a single quarter. This was up 68% from the previous year. At that time, it appeared that Teradyne's sales would reach $60 million by the end of the year making it the world's largest semiconductor equipment supplier at the time. But these projections were soon to be wiped out by a new business downturn in 1974. It was to be one of the worst downturns in component test equipment history.

By 1976, the industry had recovered from this recession and total industry sales reached a new high of $102 million. The industry was again becoming competitive. The Fairchild Test Systems Group began a renewed drive for leadership that thrust it back into the industry's top position in test. So by 1979, it had again emerged as the number one company in sales, not only in test, but also among all semiconductor equipment manufacturers. Fairchild sales for component test systems had reached $111 million by 1979, making it the first semiconductor capital equipment company to pass the $100M mark in annual revenues.

The cleaving of logic testing into two segments was another important aspect of the post 1975 competition. Microprocessor test equipment emerged as a separate branch in late 1975, with the founding of Megatest Corporation. Prior to this, in the early years of microprocessors, this segment of the industry was serviced by general purpose digital IC testers. The market for microprocessors was too small to attract major new equipment designs.

In the early seventies, demand for memory devices was exceeding demand for logic devices in ratios greater than twenty to one. Immense pressure was placed on semiconductor test equipment manufacturers to solve the memory testing problems. Consequently, machines developed at that time tended to have features that favored memory testing.

But microprocessor test requirements differ significantly from those of memories, and from those of most other logic devices. Memory testing relies upon repetitive and fairly straightforward addressing schemes. Data output from a memory is usually available in the very next clock cycle after it has been put in. Microprocessors, on the other hand, operate from a set of functional commands. These commands are not usually developed from straightforward address sequences. Moreover, the data at the output of a microprocessor might not become available until many clock cycles after it has been inputted. This gives rise to much

more complex test sequencing and test clocking schemes than is required for memories.

Therefore, in the early years of microprocessors, substantial effort was being expended to adopt existing digital test systems to the testing of microprocessors. Consequently, the larger manufacturers invested in equipment modifications and innovations, rather than in specific equipment to suit the needs of microprocessor manufacturing lines.

By 1977, test systems had become very complex. Each pin being tested by the DUT [device under test] was backed up with an enormous amount of electronics. This came to be known as the pin electronics, and the PC board upon which it is mounted came to be known as the pin electronics card. Figure 3.3.1.1-4 shows a symbolic schematic of the card. The entire card and its associated drive circuitry subsequently came to be known as a 'channel', so a tester capable of testing 256 pins was said to have 256 channels. But it was soon recognized that the channel performed dual functions—both that of being a driver and that of a comparator. So a 256 pin channel could really serve 512 pins if these were separated out. Hence, most large testers are specified either as single or as dual channel systems according to their pin electronics card's capability.

Also, by the mid-seventies, the test signals that could be transmitted and received through the channels had become very complex, even though they were still digital in nature. Figure 3.3.1.1-5 depicts the kinds of digital timing signals that are used.

In 1978, Fairchild Test Systems Group introduced the Sentinel (Series 10) test system. This marked the beginning of a new era in microprocessor testing. The equipment was evolving to a more general purpose nature in order to meet the increasing complexity of new microprocessors. The microprocessors at this time had several different types of circuits on the chip. They often consisted of on-chip RAMs, masked ROMs, EPROMs and programmable logic arrays. Such complexity requires general purpose testing capabilities. The Series 10 machine was therefore quickly accepted by the industry.

By 1979 it had also become clear that a new generation of general purpose logic testers was called for. The need for this new generation was predicated upon issues concerning design-for-testability. It would eventually become known as the VLSI tester. This had, in turn, been predicated upon scan-set testing. The overall impact caused major changes in both test equipment and computer aided-design (CAD) equipment. Testability issues centered around two manufacturing requirements: First, the requirement to quickly ensure testability; second, the requirement to reduce programming and test time. One objective of design-for-testability has been to improve productivity through better design and through better utilization of testing resources. Another objective has been to limit the rapid rise in testing time that occurs because of VLSI.

Scan-Set testing emerged as a result of immense pressure for new kinds of testing that was being generated by the computer market. This was due to the impact of the large main frame computer producers such as IBM, Honeywell, and Sperry/Univac. Scan-set testing evolved under several names. At IBM, it went by the rather esoteric name of LSSD, meaning "Level Sensitive Scan Design." At other places it is called either scan-set or "Scan-Path". What it involves is on-chip testing–meaning designed-in test circuits right on the chip itself–and totally restructured test systems.

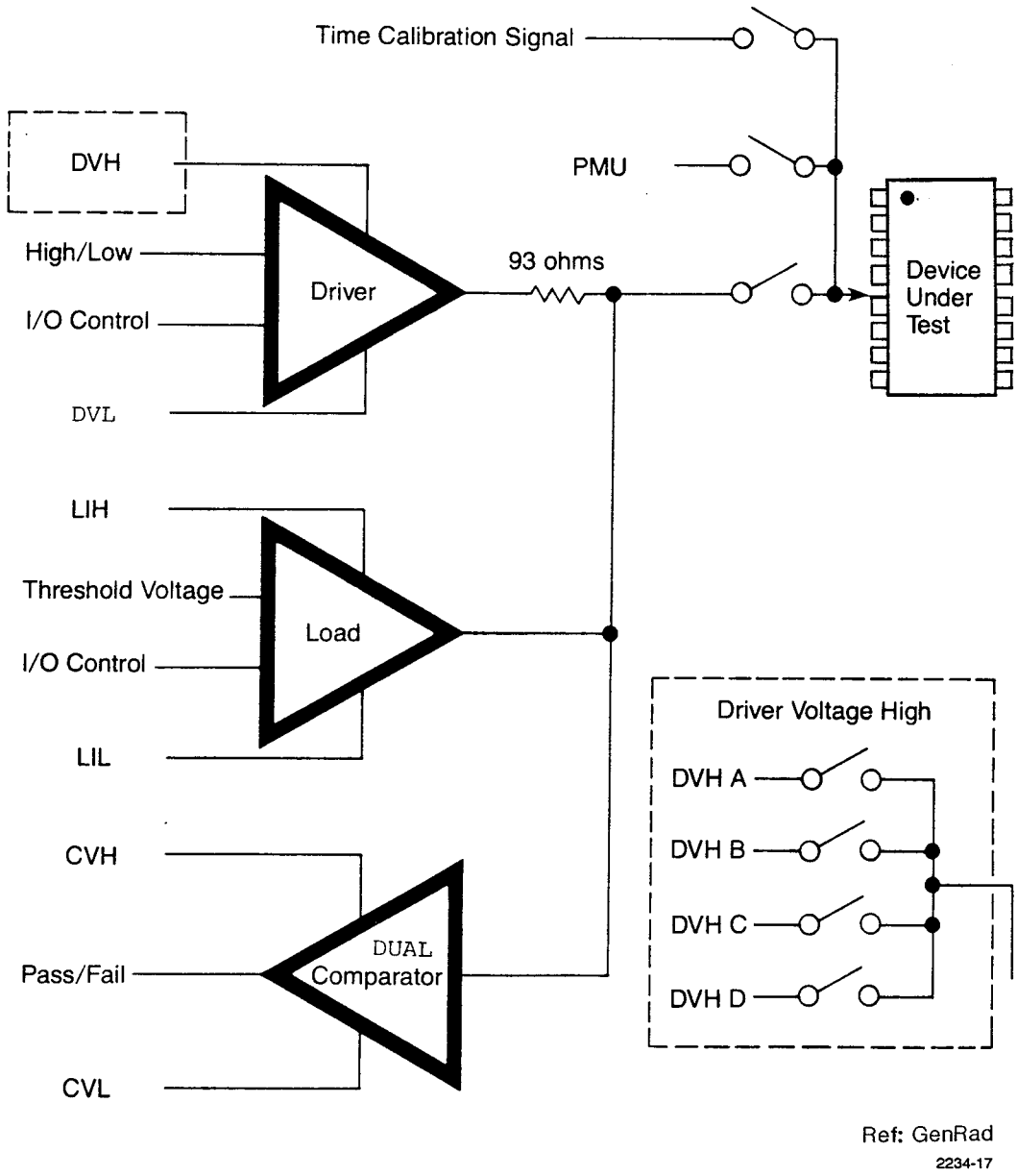
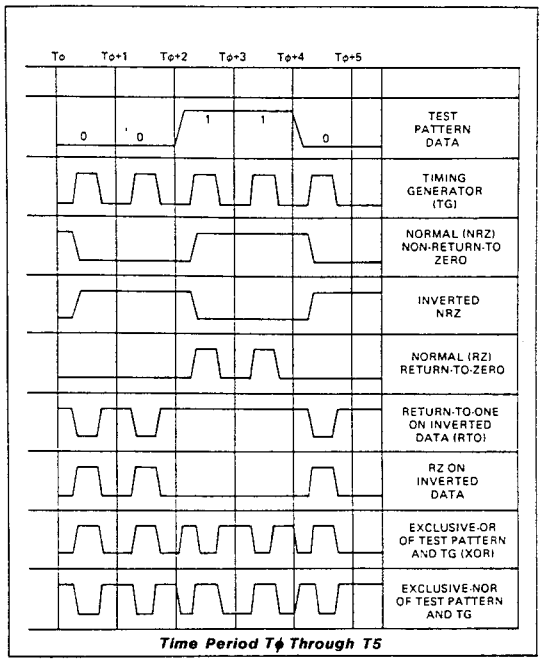


Figure 3.3.1.1-4

Typical Test Head Pin Electronics Cards



Ref: Healy, *Reston Publishing*, "Automatic Testing and Evaluation of Digital Integrated Circuits"

2234-18

Figure 3.3.1.1-5

Tester Waveforms

Development of Memory Testing

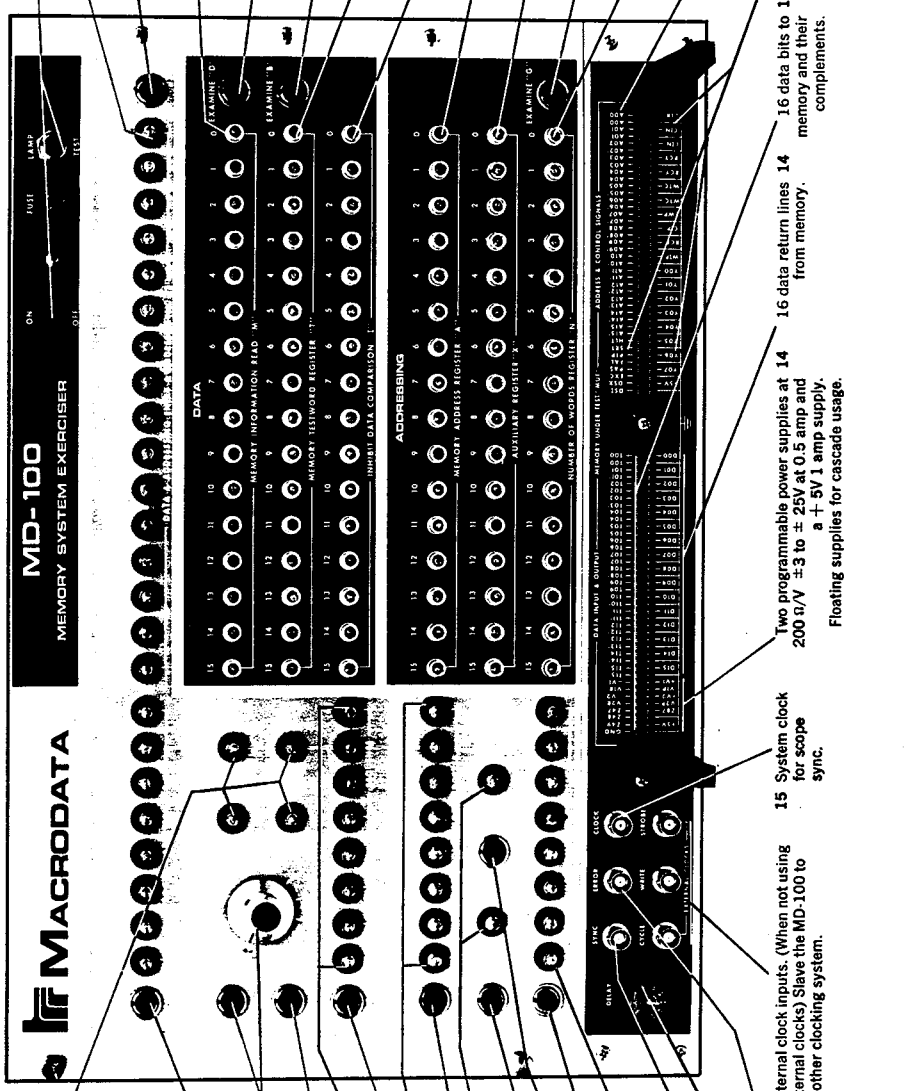
Memory testing of semiconductor components dates back to the late sixties. J-K flip flops and long shift registers had begun to be produced and tested in fairly large volumes. In addition, some small memories were emerging as well. In 1969, Intel introduced the 1101, a 256 bit dynamic RAM. By that time also, digital logic testers had begun to incorporate long recirculating shift registers into the test head to steer the driving circuits. However, this approach was cumbersome for memory testing. Industry pressure was directed at having a true pattern generator capable of changing patterns on-the-fly.

E-H Research Laboratories was one of the earliest suppliers to provide such pattern generators. However, the most widely accepted generator was the Macrodata MD100, which was introduced in 1971. It was to become the standard bearer around which the entire industry would rally. A picture of MD100 front panel is shown in Figure 3.3.1.1-6. The Teradyne J384 also was marketed at about this time.

In the seventies, the market was characterized by rapid evolution in tester complexity and capability. Memory testers emerged as a separate branch of IC testers. Memory applications were growing so rapidly that demand for semiconductor memories drove the memory tester market to very high growth rates by the mid-to-late seventies. Market growth for memory systems sometimes exceeded 75% per year.

Teradyne and Macrodata were the two major players in memory testing during this period. But by 1974, Teradyne had captured the major market share from Macrodata–about 36%. Its 1974 sales in memory component testers stood at $6.0 million. Macrodata was then number two with $4.5 million in sales and a 27% market share. More than a dozen other companies scrambled for the remaining 37% of that 1974 market.

Exceptional market demand for memories accelerated the memory tester market to a peak market share of about 28% by 1978. Memory testers had undoubtedly become the fastest growing segment of all automatic component test equipment. But this picture faded in the early eighties due to strong competition and to rapidly increasing test times. Test economics had become the primary issue, thus the industry was plagued with price cutting. American semiconductor companies took the tact of buying lower cost testers. Japanese manufacturers took the tact of buying more expensive, but more productive parallel testers. These strategic



Ref: Macrodata MD-100
2234-15

Figure 3.3.1.1-6

The Macrodata MD-100 Memory Systems

decisions played a significant role in the strong shift of memory device market to Japan.

Greater productivity of capital was the lever Japan used to become the world leader in semiconductor memories. Japanese customers did not believe that the low-cost testers as an answer to test economics. In contrast, they focused on test quality and upon parallel testing for productivity. This philosophy resulted in surprising competitive displacements, in increasingly international sales demographies, and in a strong emergence by Japanese test equipment suppliers.

With Japan's thrust into the memory market, American dominance of the memory tester market quickly shifted to favor Japanese equipment suppliers. Takeda Riken (since renamed as Advantest) emerged as the largest supplier of memory test equipment in 1981. Teradyne was one of the few American companies to recognize the shift to Japan. Teradyne managed to successfully implement niche strategies. In the U.S. it focused on memories other than DRAM's and on supplying captive manufacturers. Meanwhile, it invested heavily in Japan, shifting some manufacturing and design there.

Development of Linear Testing

During the late sixties, linear automatic test systems were emerging as well, and it too had its roots in logic test systems. Linear IC test methods grew directly from the application of logic testers to the testing of operational amplifiers. Virtually all original linear IC's were operational amplifiers. Linear integrated circuits were first shipped in volume in 1966. But a mere 2.3 million units were shipped that year. However, by 1968, shipments had jumped to 18 million units and the linear IC industry was feeling the pressure for a good tester.

The strong trend in operational amplifiers and voltage regulators continued well into the early seventies. This rapidly increasing complexity of linear integrated circuits propelled the linear device industry through three phases of circuit types and consequently through three stages of testers. The first stage might be described as the operational amplifier era. During this period, circuits such as operational amplifiers, comparators and voltage regulators were brought into operation. The circuits drove the linear tester market of the early seventies.

During these early years, demand for linear test systems favored operational amplifier testers so strongly that the linear test equipment market never developed a broader line of testing capability. Operational amplifiers, comparators and voltage regulators could all be tested conveniently with digital test methods, provided that the user was willing to design a 'linear test adapter box' for each and every linear IC product line he wished to test. Machines such as the Fairchild 4000 and the Fairchild 5000C did an admirable job for this, so long as the linear IC to be tested was imbedded in that box, and provided its outputs could be read by the digital test equipment as voltage and current parameters.

Eventually the 'box' terminology was dropped and the circuitry came to be known simply as a 'linear test adapter'. When a digital machine is used in this fashion, its main function becomes merely that of acting as a programmable power supply source, a programmable measurement system and a software data converter. The major digital test portions of the system usually are left unused.

From a testing viewpoint, the op amp era focused linear test issues directly away from the digital controller and its associated relay switching matrix and onto the linear test adapter itself. The issue to resolve became

one of how to imbed the linear circuit into such a digitally controlled matrix.

Three approaches were taken. Fairchild offered its digital systems as mentioned above, but left fabrication of the linear test adapter to the customer. A few specialized testers were made between 1978 and 1980, but these consisted of nothing more than a specialized linear test head. Next, Teradyne introduced the J273. This was a totally integrated system that contained the linear test adapters along with the rest of the automated test system. This system represented the first true advance in linear test systems design. Unfortunately, the linear test adapters were in the mainframe and could only be accessed via a long cable. This type of architecture is referred to as a hybrid test head architecture. All other companies at this time were offering specialized bench top equipment. These benchtop testers were dominantly nothing more than just a single linear test adapter with a few extra control circuits and power supplies.

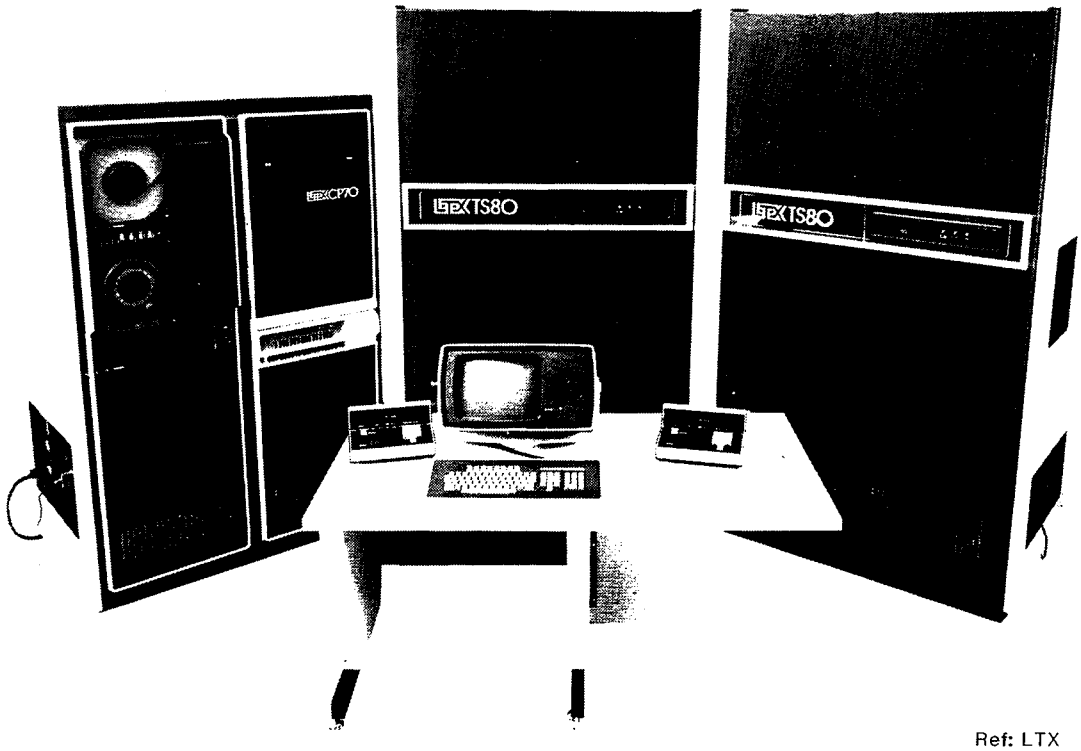
During this period, Teradyne was the only company offering a machine that was generally acceptable to the industry. By 1977 Teradyne had captured 74% of the linear testing market. Fairchild was then number two, with about 25% of the market.

Nevertheless, events had already been set in motion which would displace the dominance of these two companies. The second phase in linear circuits combined both analog and digital functions in a single chip. Digital to analog (D/A) converters began to appear in the early seventies. Frequency-to-voltage (F/V) and voltage-to-frequency (V/F) converters were also introduced by 1975. By 1977, the dam had burst for demand for totally new machines to test these circuits.

Teradyne and Fairchild were slow to respond to the market place. The market for testers with both digital and analog test capability was then too small. Consequently, most of the first generation of analog-digital testers were custom built. These custom units included some analog instruments, a digital clock, and the use of a golden device against which to compare. But these testers offered only simple comparisons between the DUT and this so-called golden device. The tester itself could only provide simple pass-fail answers. No grading parameters were obtained. More importantly, there was no guarantee that a complete test of the device was performed.

A second generation of linear testers incorporating standard digital testers and specialized analog instrumentation was designed. This approach provided better analysis of signals. At the same time, analog test manufacturers merged digital test capability into their testers. However, neither of these testers had the capability to analyze cross-characteristics between the digital and analog portions of the circuit. The systems needed digital signal processing capability in order to do this. Such capability would allow conversions of all analog signals into digital code. This gave linear engineers an additional benefit: digital test programming methods could be applied once all testing was done in a digital format. Key parameters and measurements could now be changed by simply changing the program. These issues laid the foundation for the third generation of linear testers.

In 1977, National Semiconductor contracted for a custom design of such a linear tester from Lorlin Industries. Simultaneously, a group of key linear design engineers left Teradyne to form LTX. LTX was the most innovative of the two, and so, soon came to dominate linear testing. LTX was the dominant force in linear testing throughout the eighties. Its MTS77 is probably the longest lived system to maintain market dominance in the history of the semiconductor equipment industry. It is shown in Figure 3.3.1.1-7.



Ref: LTX
2234-16

Figure 3.3.1.1-7

The LTX MTS77 Modular Automatic Test System

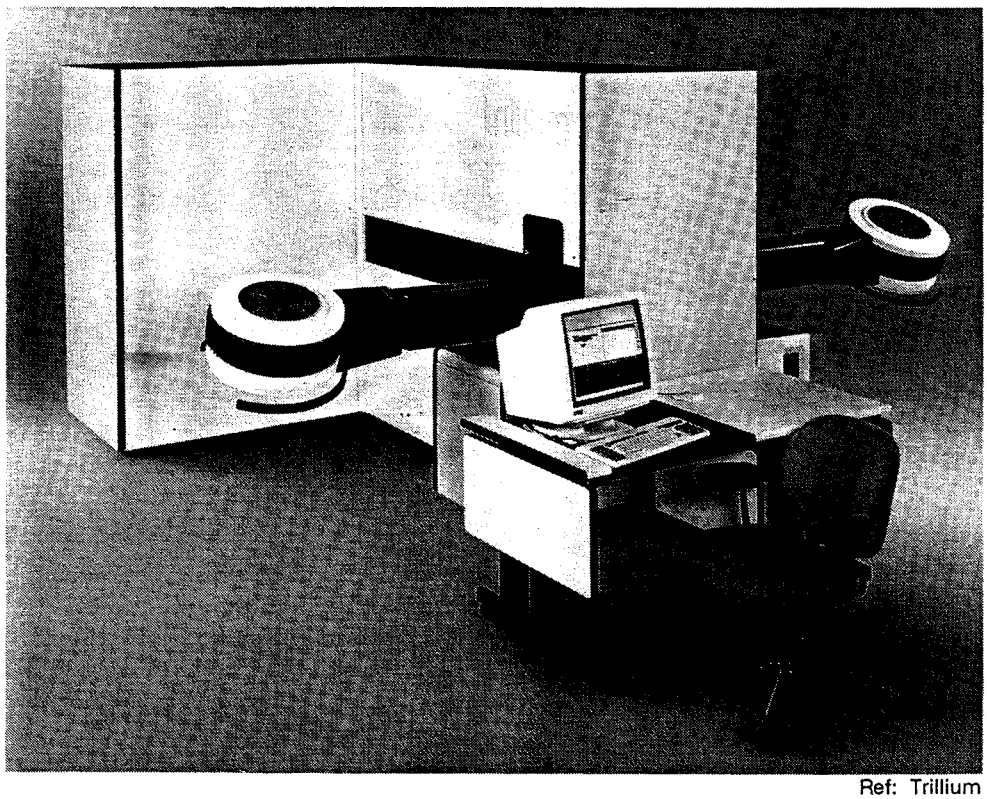
The Eighties

By 1981, it had become clearly recognized that VLSI testing was not just a more complex form of LSI testing, but it was a new methodology as well. Three things were different about this approach. First, at IBM, several chips were mounted on a ceramic substrate much like a hybrid circuit. Second, as mentioned previously, scan-set test methods are used. Third, fault diagnostics were also used. Consequently, all of the complexities of board level testing were added to those of component level testing. A few of these complexities are: (1) The wafer prober began to take on the work of an upside-down bed-of-nails tester. (2) The pin count and probe quantity increased enormously–several hundred probes were not unheard of. (3) CAD/CAT (Computer-Aided Design/Computer-Aided Test) was essential. A high speed data bus back to the main computer became an integral part of the system. (4) Automatic test sequence generation, fault simulation, fault diagnostics and fault location procedures were essential.

In essence, as VLSI testing evolved it came to contain board test methods, component test methods and fault generation routines all tied up into one highly integrated large-scale system approach. It was, and is, true VLSI testing.

By our measure, the three essential elements that came to differentiate true VLSI component testers from their general purpose LSI predecessors were namely: a tester per pin architecture, a workstation environment, and a high speed data bus. Additional equipment feature changes that evolved to accommodate these essential elements included: Asynchronous clocks, On-the-fly I/O switching, 256 to 512 pin capability, 40 MHz to 100 MHz clocks, structured program languages, High speed–on line–mass memory and test procedure controllers.

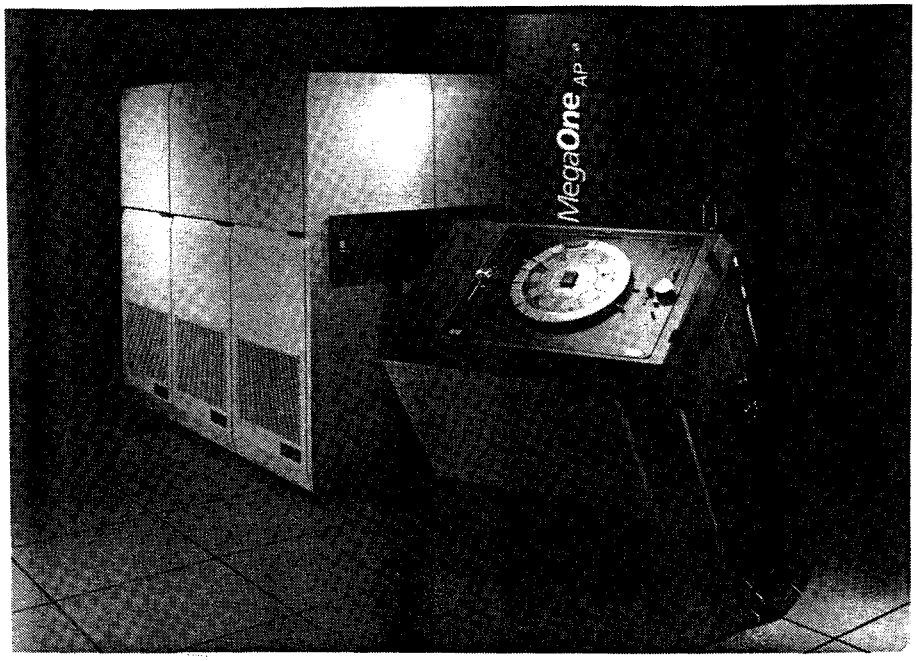
The VLSI test equipment market did not prove easy to enter. It bankrupted Accutest. GenRad planned to expend $20M for its start-up, but actually spent more than $40M. Most of the early start-ups were not successful in this new market, the only exception was Trillium. Trillium was started by a team that left GenRad which had previously left Fairchild. It was this design team's third effort at a VLSI tester and it proved to be enormously successful. Trillium pioneered the use of engineering workstations in testers. (See Figure 3.3.1.1-8). They also borrowed the tester-per-pin concept from Megatest. The combination of these two technologies enabled them to be the only successful VLSI ATS start-up. This also brought LTX into the logic segment through its funding of Trillium. This would later prove invaluable to LTX when they entered mixed signal testing.



Ref: Trillium
2234-63

Figure 3.3.1.1-8

Trillium's Micromaster Workstation



Ref: Megatest
2234-64

Figure 3.3.1.1-9

Megatest's MegaOne Automatic Test System

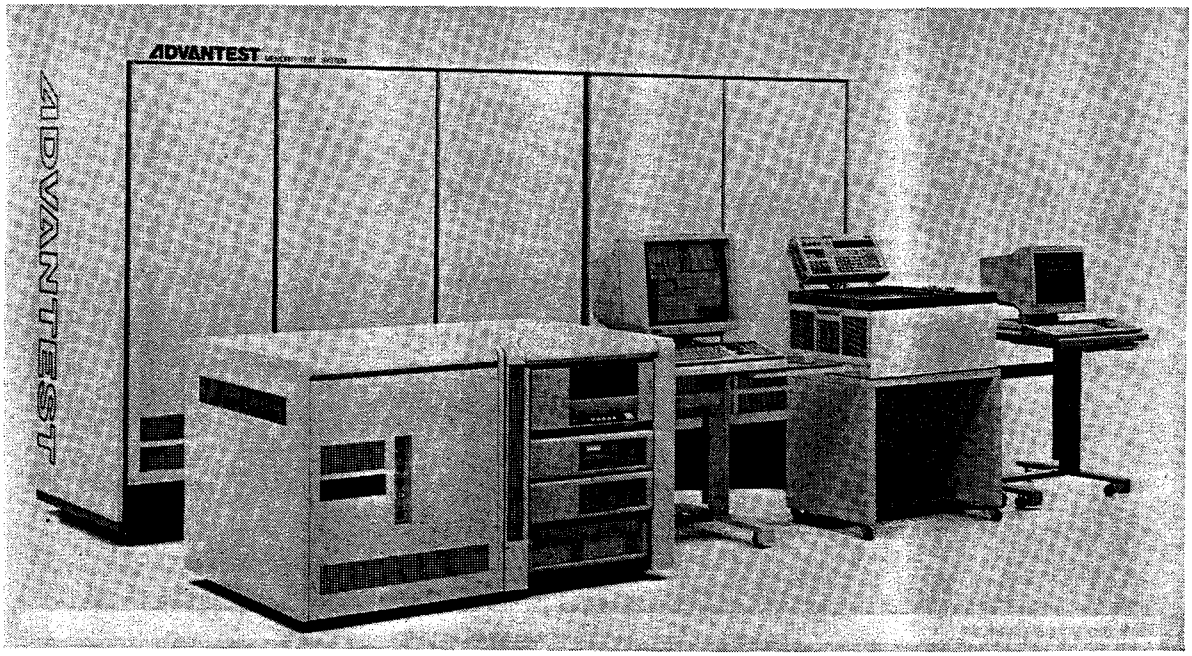
While not a start-up, Megatest was also critical in the development of VLSI ATS. Megatest pioneered the tester per pin concept with its Megaone™. (See Figure 3.3.1.1-9). At the time, Megatest was a small supplier of dedicated systems with a reputation for youthful innovativeness. Many considered them to be the 'Apple' of the ATS market. Like Apple, Megatest was faced with the problem of overcoming the popularity of its first system. Like Apple's MacIntosh™, the Megaone established Megatest as a serious top contender and its tester-per-pin architecture forever changed the way in which engineers thought about test systems.

Meanwhile, a more potent threat emerged from Japan. Japan's VLSI program of 1976 pushed Japan into the forefront of shared resource tester technology. Advantest (formerly Takeda Riken) pioneered the emergence of high speed and high pin counts. This was extremely critical for American captives. Consequently, between 1979 and 1982, American logic test system manufacturers suffered a sharp drop in market share, from 85% to 67%. Japanese manufacturers supplied virtually all of the remaining 33% share. Fairchild lost its dominant position and Advantest became the largest supplier of logic test systems in the world. It had emerged from virtual anonymity in only five years to surpass most American companies, as well as its Japanese rival, Ando.

The Japanese's strength in logic testers carried over into their memory test systems.

This strength caused a dramatic shift both in market segmentation and in memory equipment architecture.

In 1983, 64K DRAM prices stood at about $5.00. By 1984, they had dropped to 60¢. This market movement to Japan was a direct result of Japanese manufacturer's commitment to the memory market. They invested heavily in high volume plants that were dedicated to DRAM memory production. As a result, these plants were much more cost effective than were those in the U.S. This proved to be a bonanza for Japanese test equipment suppliers in the mid-eighties. Figure 3.3.1.1-10 depicts a modern Japanese tester from Advantest. Figure 3.3.1.1-11, 12 & 13 shows Teradyne's J937, Schlumberger's S90 and Megatest's Genesis II memory testers respectively.



Ref: Advantest
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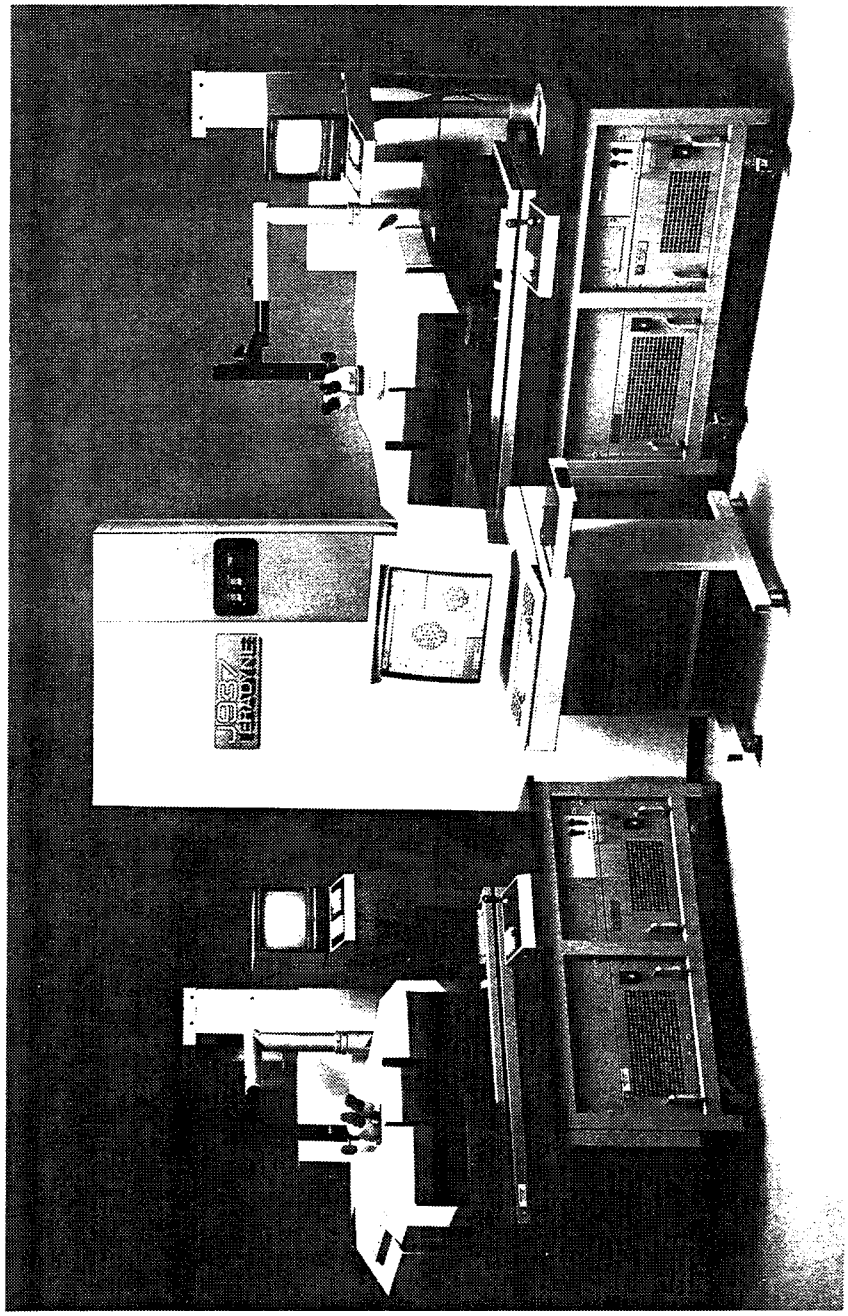
Figure 3.3.1.1-10

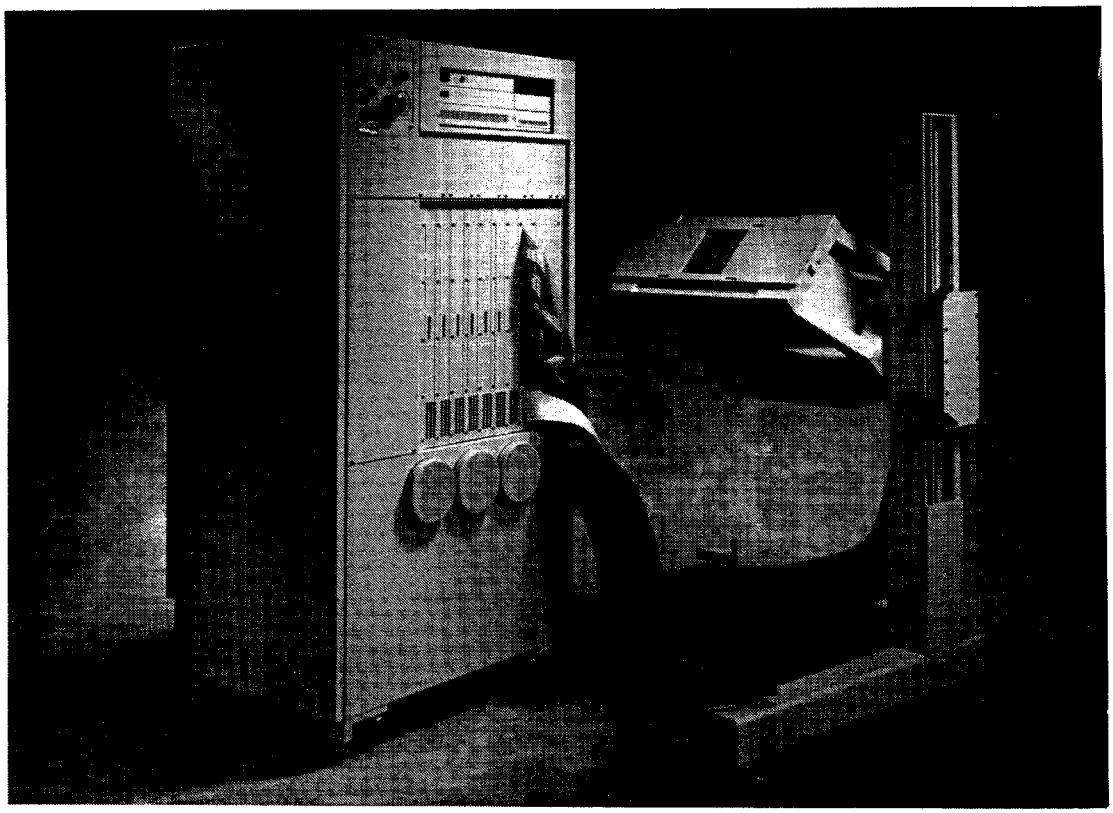
The Advantest T5381 Memory Test System



Ref: Teradyne
2234-22

Figure 3.3.1.1-11

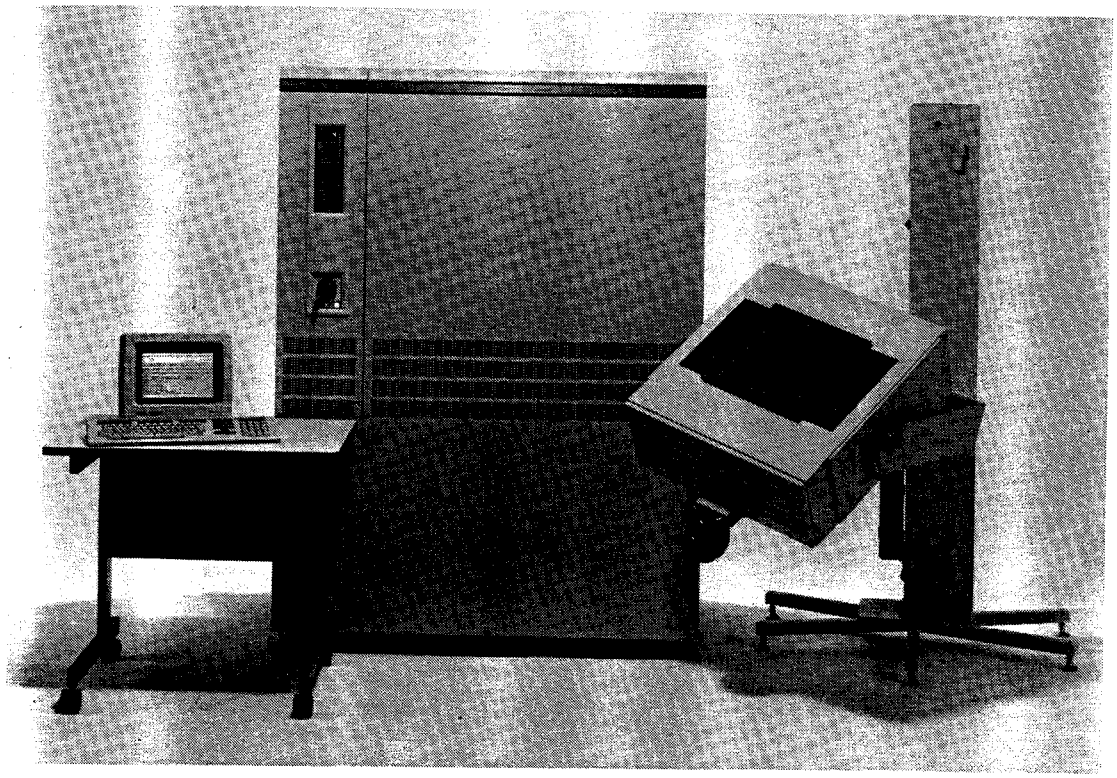
The Teradyne J937 Memory Tester with Wafer Probers and Automatic Handler for Parallel Testing up to 16 Units Simultaneously.



Ref: Megatest
2234-45

Figure 3.3.1.1-12

Megatest's Genesis II Automatic Memory Tester



Ref: Schlumberger
2234-44

Figure 3.3.1.1-13

Schlumberger's Model S90 Automatic Memory Tester

The technological driving force for memory testing is simply an expansion of the drive for increased memory capacity. This trend to move from 64, to 256, to 1 Mbit to 4 Mbit is important because worldwide memory test time demand is so dominated by DRAM's: They consume a majority of memory test time demand. Consequently, one of the few opportunities lies in the niche market for testing high speed static RAM's. Even though this market is relatively small, it is technology driven, thus it can command higher tester prices.

In addition, one of the hottest areas of memory test in the late eighties and early nineties is that for Video RAMs—or VRAMs—as they are popularly known. VRAM's were pioneered in the United States for rapid refresh of graphic displays. Digital TV also uses lots of memory. The more advanced designs can require as much as 16M bits of memory. Some Japanese companies expect VRAM's to consume between 30 and 50 percent of all DRAM production by 1995.

The need for increased memory is a result of the need for fast display updating of high resolution displays. It requires a different memory design because of the dual tasks of image updating and screen refreshing. Each task vies for the frame buffer at the same time. The display memory is stored in the frame buffer. A dual ported video RAM solves this problem. Each port has its own

memory. There is also a shift register on the chip and an unusually wide internal bus linking both RAM's. Each RAM works independently most of the time. But once a display is updated, it needs to be dumped almost instantaneously to the other RAM for screen refresh. This is why the wide bus is needed.

A typical test strategy includes all the tests common to DRAM's such as: DC parametrics, power supply current, high voltage-low voltage, functional sequential port sort test and cross talk test. Unique tests would include a clock shift range test, data hold time, verifying transfer cycle from shift register to memory array, testing tap points.

Such complexity in memory devices would appear to require a highly complex tester. And in fact, some companies are using VLSI Logic testers to test such parts. But this is a costly approach and a new generation of high speed GP memory tester is needed.

The eighties has also seen the emergence of analog-per-pin test head architecture in linear test systems. This architecture was pioneered by Axiom and Attain. These linear systems are—at-heart—mixed-signal test systems that can test both mixed signal and linear circuits. (See Figure 3.3.1.1-14)

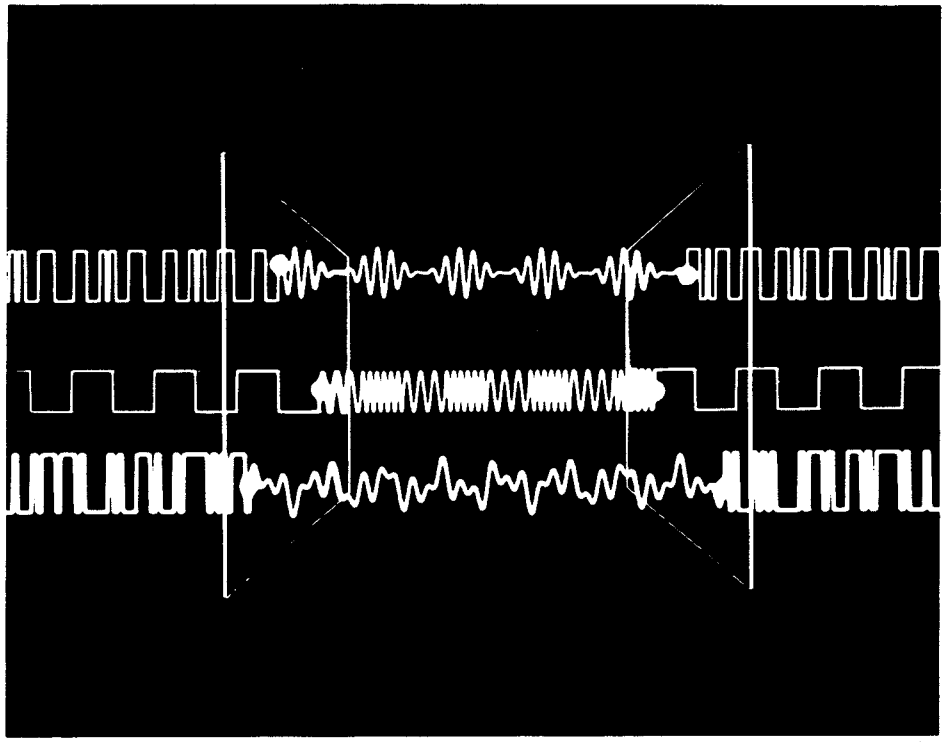
The Teradyne A500 is a mixed signal tester with a hybrid test head architecture. It is depicted in Figure 3.3.1.1-15. A brief system block diagram for it is shown in Figure 3.3.1.1-16.

Another feature appearing a most mixed signal testers is the ability to put virtual oscilloscopes and virtual spectrum analyzers on the screen's display and pull-down windows. A typical presentation from the Teradyne A500 is shown in Figure 3.3.1.1-17. The heart of Teradyne's A500 Analog VLSI Test System is the Vector Bus II, which integrates analog and digital VLSI test capability at the system level–rather than at the test head. The Vector Bus II provides system-level synchronization, mixed-signal event control and multisource data mixing.

As mentioned, the merging of digital and analog circuitry has brought about a renaissance in the linear market. A key driving force was the merging of the telecommunications market with the microprocessor market. Techniques such as digital signal processing which use microprocessors to analyze analog signals have also come into the forefront.

An example of one such application is the Modem. The need for linking computers together into worldwide networks became inevitable as digital computer applications grew. This brought to bear some of the first issues on linear applications. Originally, the world's telephone and telecommunication systems used only analog transmissions. Demand for transmission of digitized computer data fostered the need for the Modem (modulator-demodulator). Modems are used to convert digital bit streams into analog signals at the transmitting telephone. Another modem reconverts those analog signals back into a digital bit stream at the receiving end.

But demand for digital telephone transmission systems has outgrown the analog portion as the amount of computer networking has grown. Today, a large portion of all telephone transmissions consist of digital data rather than voice data. So it has become more efficient to pulse-code-modulate voice signals and to change them into digital signals rather than vice-versa. This in turn is leads to integrated digital systems, or ISDNs, as the telephone companies call them–meaning Integrated Services Digital Network.



Ref: HP
2234-23

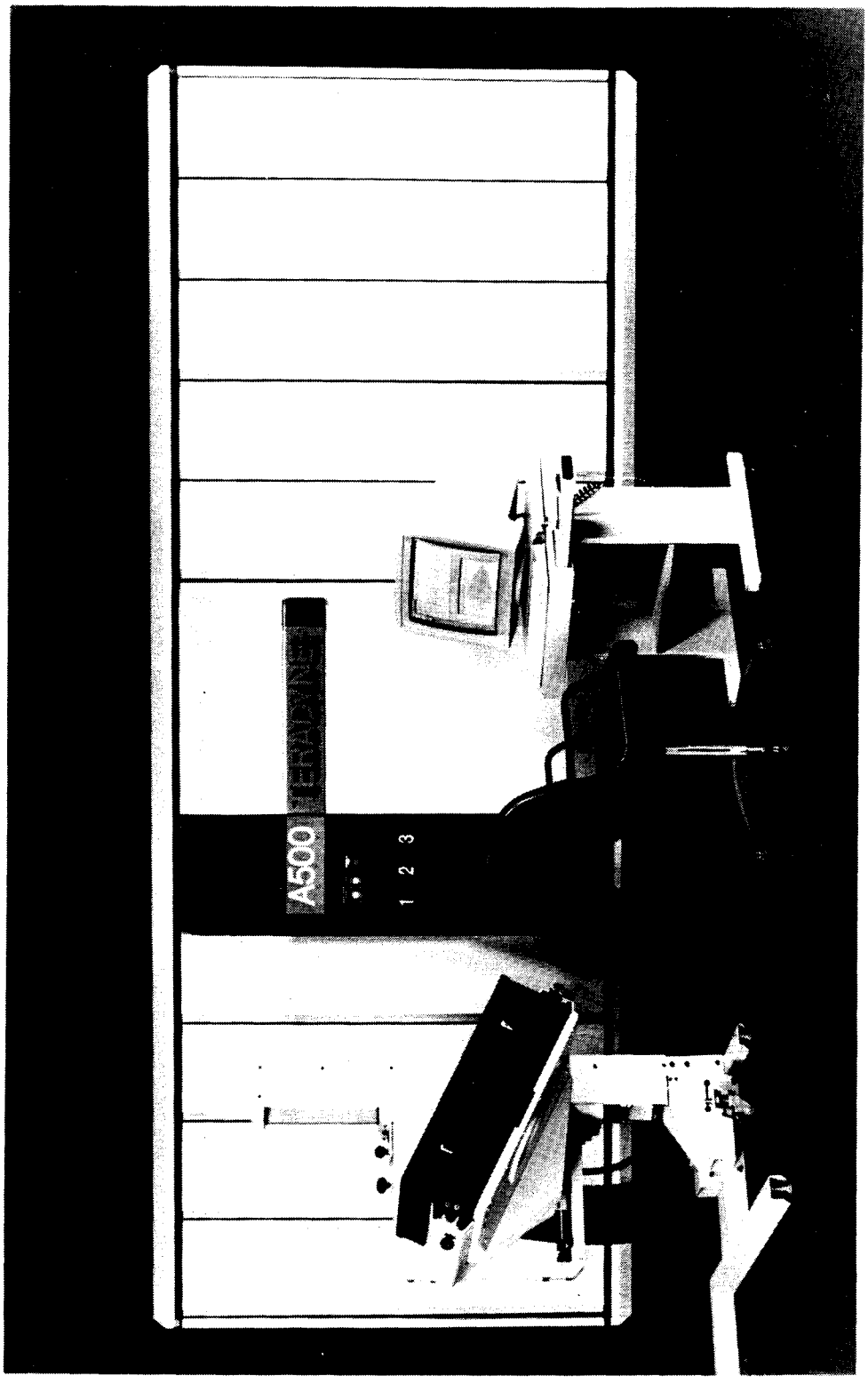
Figure 3.3.1.1-14

Mixed Signal Testers are those which can process information from circuits that accept and return digital signals while processing them as analog ones, or vice versa.

The reason for this switch to digital is related to the number of channels which can be carried over a pair of wires. An analog transmission can carry 12 voice channels on a single pair of wires. But up to 32 digital voice channels can be carried on the same pair†. Therefore use of digitized voices on existing lines would increase the capacity of America's phone system by more than two and one half times, without requiring further investment in cabling or installation. It is not surprising then, that the phone companies show such interest in digital phone systems.

There is another benefit with digital transmission systems. In an analog transmission, noise is amplified whenever the signal is amplified. So noise tends to accumulate when signals are transmitted over long lines. This does not happen as rapidly with a digital system. Digital systems thus extend the useful life of phone lines, since their transmissions can continue to be sent over the older and the more noisy phone lines.

† Martin, James, "Telecommunications and the Computer", 1976, pg. 266.



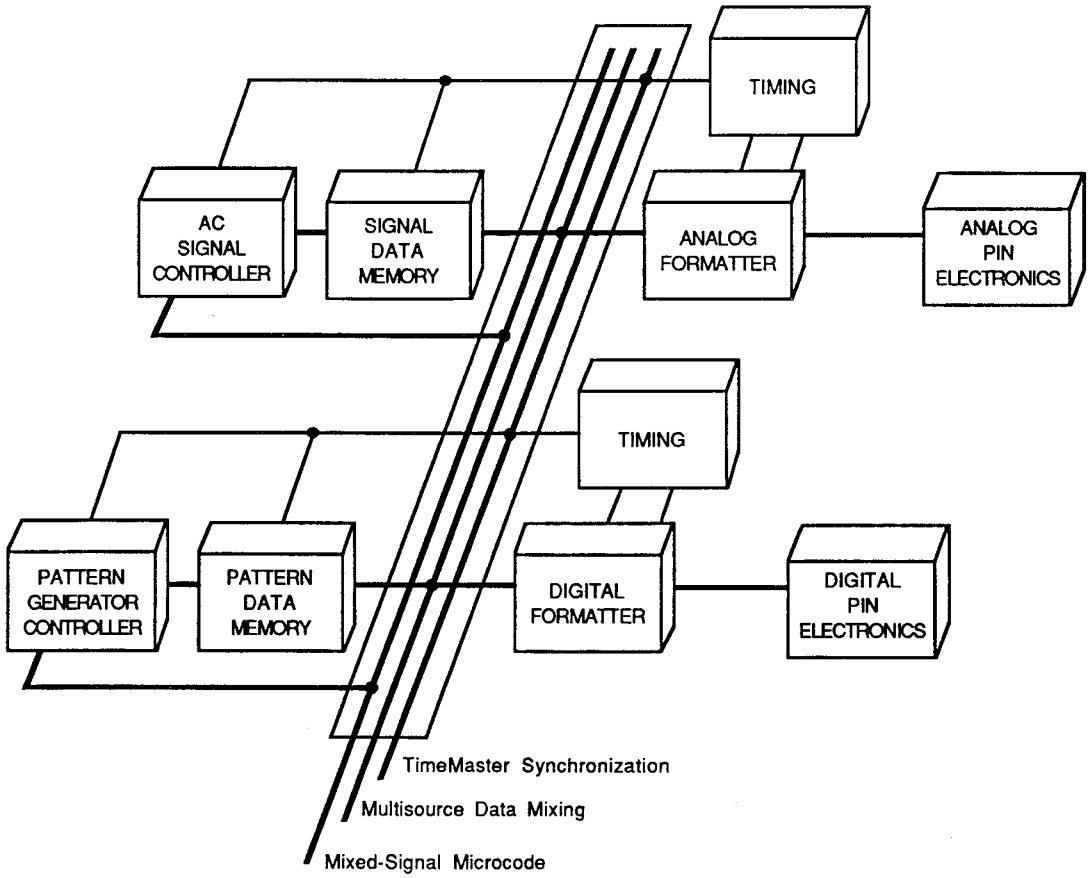
Ref: Teradyne 2234-25

Figure 3.3.1.1-15

Teradyne's A500 Analog VLSI Automatic Test System

Figure 3.3.1.1-16

VECTOR BUS II™ ARCHITECTURE OF THE TERADYNE A500



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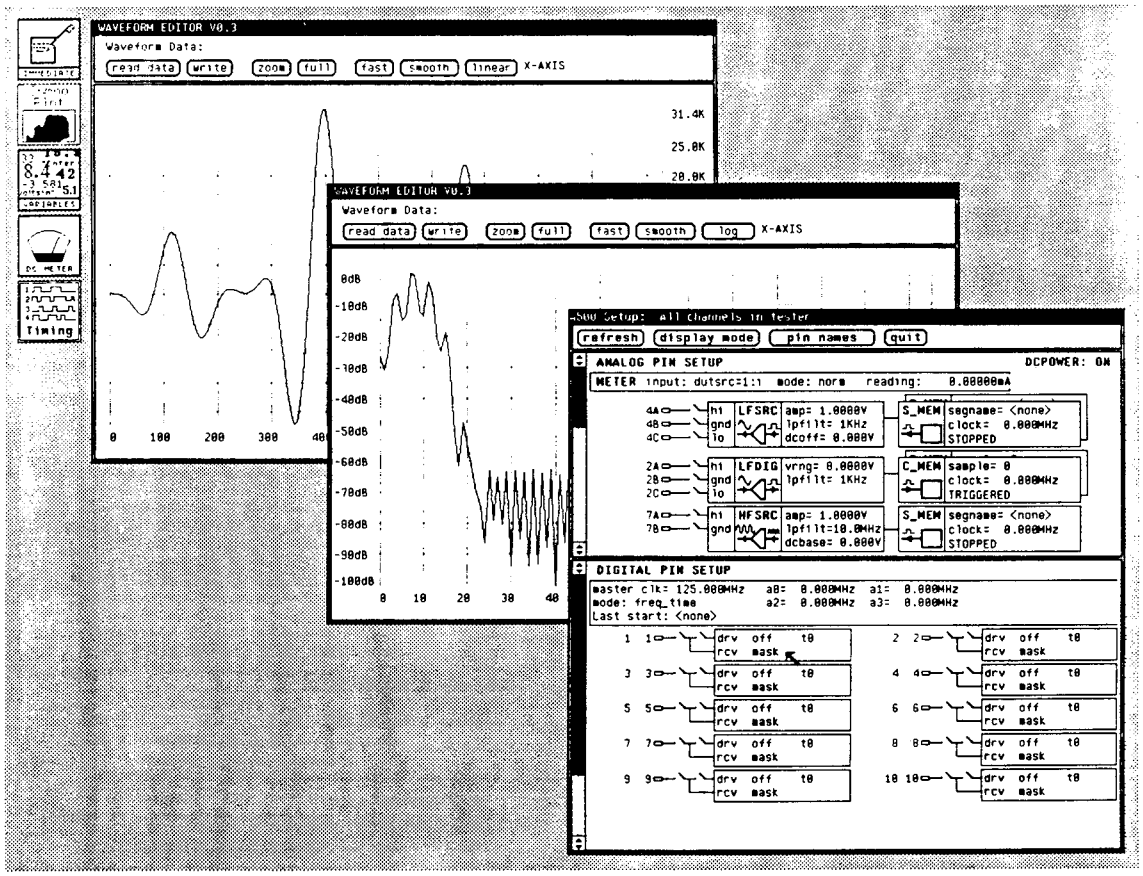

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Figure 3.3.1.1-17

Virtual Oscilloscope Display Via Windows on the A500

The analog signals might become buried in noise on the same type of line.

Recent introduction of U-interface integrated circuits provides the last link in achieving a complete integrated services digital network. This will now make it possible to have new applications for both customer and telephone company equipment. The U-interface connects the user's communications device with the telephone company's central office switching equipment and allows the user to accomplish full ISDN transmission for the first time.

Implementation of digital networks has also generated a need for another communication circuit called the codec (coder-decoder). Codecs are used to convert analog signals into digital signals for digital systems. With digital systems, each phone must have a codec in order for it to function properly. Codecs perform the inverse function of modems. They convert analog signals into digital codes. This is accomplished by using Pulse Amplitude Modulation (PAM) and Pulse Code Modulation (PCM).

Pulse Amplitude Modulation consists of chopping a signal into tiny increments of time, and then encoding the signal into a series of digitized pulses. Since the amplitude range of the pulses is continuously variable, they are still in analog form, not digital. They look like a sawed up version of the original sine wave or digital code. The next step is to pulse code modulate (PCM) each PAM signal. PCM offers the advantages of reducing the total number of bits needed to transmit the signal. Only limited samples of the total PAM signal need to be coded in order to faithfully reconstruct the original sinusoids at the receiving end. Consequently, the bit streams from several PCM sinusoids can be compacted into a length that is similar to that of single PAM signals from the original signal. This offers an economic benefit by speeding up data transmission substantially as well as compacting the total signal.

Another important category of circuits driving mixed signal testing is integrated signal processing (ISP). These devices were originally developed for telephone use, but have found many other applications. Speech synthesis is probably the most common application. An increasingly important application of integrated signal processing is in the video area. The important devices are D/A and A/D video processors and video palettes. The demand for high quality graphic capabilities will continue to put pressure on improvements in these devices. Further, as multimedia applications begin to emerge, the market for testing video mixed signal devices will grow tremendously.

The markets for digital signal processing (DSP) and embedded controllers will also drive the need for mixed signal testing. Growth of the DSP market is driven by the greater performance and flexibly offered by these devices. Embedded controllers provide the ability to design in high levels of integration which lead to increased speed and reduced system size.

Yet, testing ISP devices have proven to be difficult. Major issues at the linear circuit component level have concerned cost, speed and integration ability. High levels of integration in semiconductor manufacturing offer tremendous improvements in cost and speed. Previously, ISP has been too costly to implement at the systems level. Their use was restricted to those user segments which were cost independent. Additionally, such systems were slow, which barred them from many real-time applications. Automotive and speech synthesis applications were unrealistic. However, these limitations have fallen away as the level of integration has been increased. Consequently, entire ISP systems can be integrated on a single chip.

The Economics and Value of Testing in the Eighties

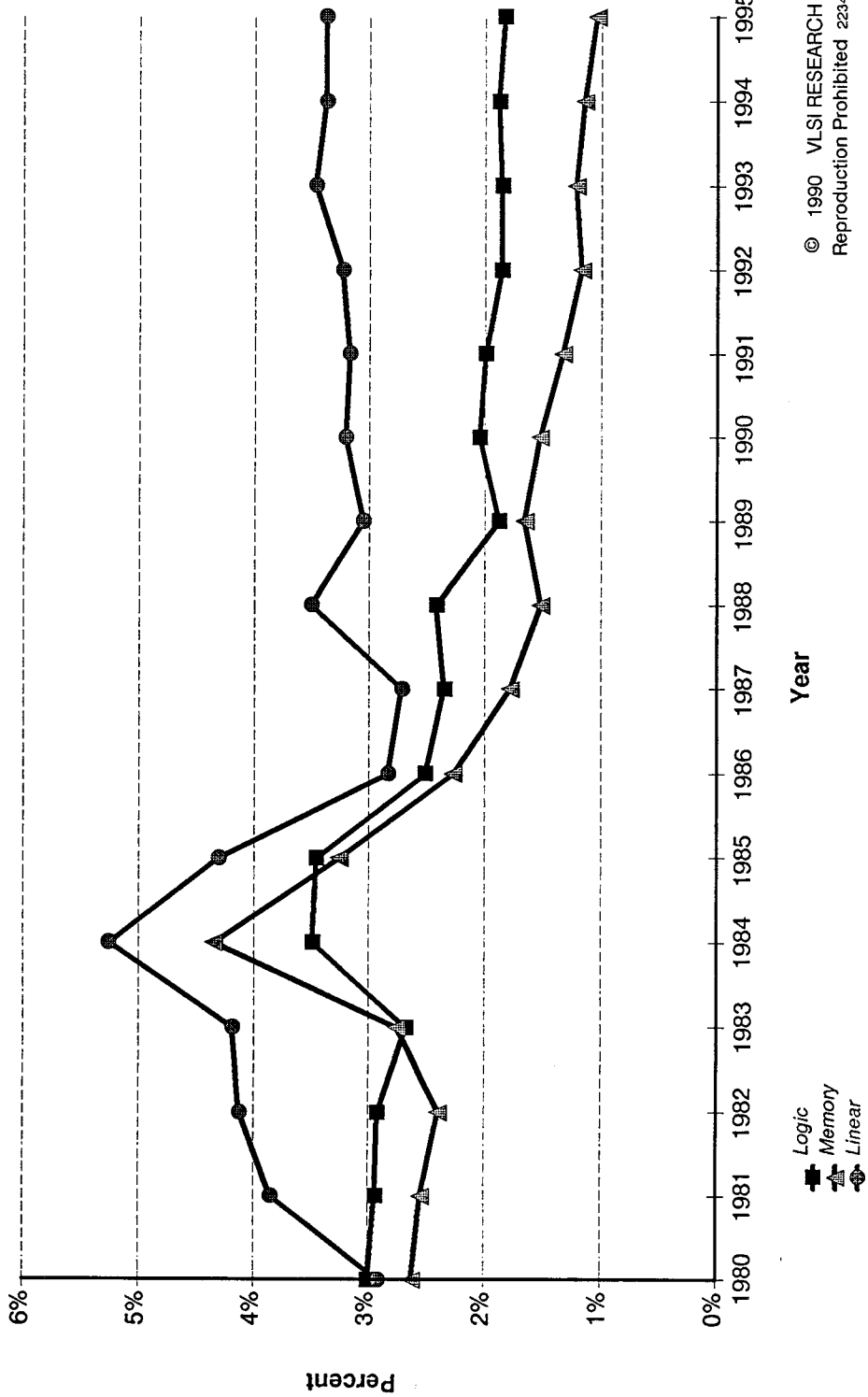
One of the most perplexing trends to occur in the ATS industry during the eighties has been the decline in market growth. The CAGR 12.8% experienced by ATS in the eighties was less than half that of the previous decade. The impact of this can be seen in Figure 3.3.1.1-18, which shows the percentage of semiconductor sales spent on ATE equipment in the eighties. Clearly, less is being spent.

There are several reasons for this. One is that expanding capital costs in wafer fabrication forced the industry to be more frugal with its capital dollars. However, this does not mean that successful companies have bought cheaper testers. Instead, they have bought more productive testers. Overall, system productivity has increased faster than price resulting in an ability to cut capital costs in testing. The ATS industry has done a marvelous job of getting greater productivity out of each additional capital dollar spent. This productivity came from faster test speeds, reduced dead times during testing and the development of

Figure 3.3.1.1-18

ATS BUYING RATE TREND

(as a percent of semiconductor sales)



parallel test technology. The results were that, tester prices went up by at least four times, device complexity went up by eight times during the eighties, yet capital expenditure rates were halved. This was a great success story for the ATS industry.

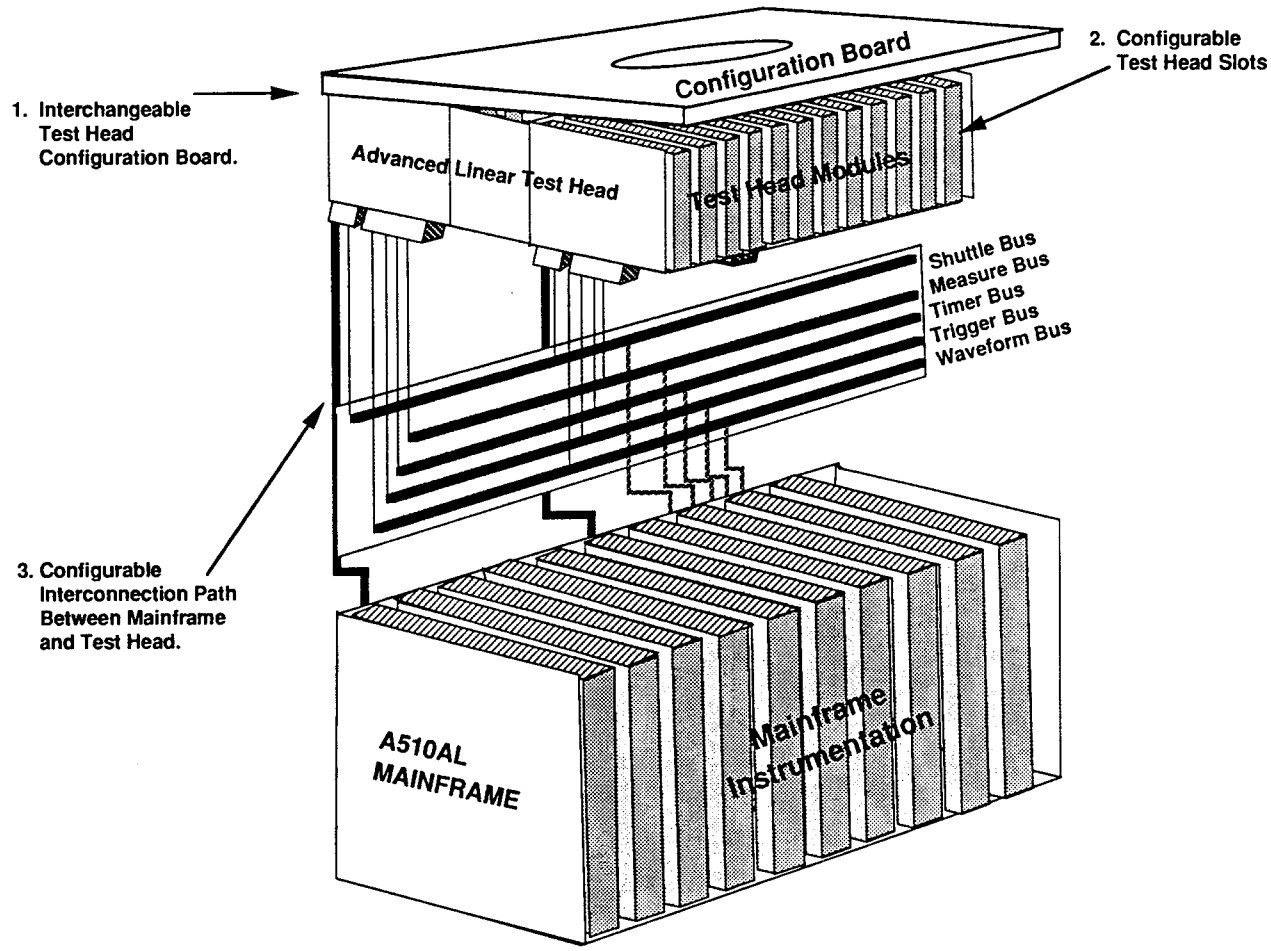
Still, users continue to demand more efficient systems at a low cost. The solution to this dilemma has been the advent of scalable, or configurable architectures. One such system is the Teradyne A510AL. Like most scalable systems, this is a user-configurable system that offers high performance and can be easily expanded to accommodate future improvements in device performance.

Figure 3.3.1.1-19 shows how the A510AL is scalable at three levels. At the top level is a configuration board which routes signals from test head modules to the device under test. Teradyne offers a series of these boards from which the user can select the appropriate units. Below the configuration board is the test head itself. Most of the test head modules can be custom-configurable making them easy to change as the user's requirements change. Finally, signals travel from the mainframe instrumentation and the test-head and configuration board to a set of user configurable buses. Other systems such as LTX' Synchromaster have a similar scalable architecture.

Another factor affecting the decline in ATS growth rates was the continued increase in probe yields and its effect on the value of testing to semiconductor manufacturers. Figure 3.3.1.1-20 will help illustrate what happened. The figure shows that there is a peak value of testing when manufacturing yield hovers around 50%. To see why, it must first be acknowledged that the value of testing is permanently wedded to manufacturing yields. Let's distort the argument to the point of absurdity so as to bring out the cause: If one absolutely knew in advance that the components to be tested were going to be good, there would be no need whatsoever to test. No additional knowledge could possibly be gained so the value of testing would be zero. Likewise, if one knew equally well in advance that a part was to be defective, the value of testing would again be zero. Consequently, testing only has substantive value when manufacturing yield is neither zero nor 100%. Now, simple binomial statistics can be used to show that the uncertainty, and therefore the value of testing reaches a parabolic peak when long-term manufacturing yield is 50%. As yield approaches the limits of either zero or 100%, sampling methods come to prevail over in-line, 100%, testing. And sampling tests are only there to ensure that the process works, not to show whether the device is good or bad. For if the process passes, the device will surely pass.

Now look what has been happening to yield (Figure 3.3.1.1-21). Die-sort yield has become the major weed-out point of manufacturing-related defects. Industry-wide manufacturing die sort yields have risen from typical values of 10-15% in the sixties to today's values of 75%. SSI components now yield around 99%. Japanese die sort yields of 256K DRAM's are reported to be near 100%. Final test yields show similar improvements. Today's final test yields seldom drop below 95%. Meanwhile, line yields have risen to values around 95%, up from their 1970 range of about 60%. These improvements are the driving pressures that have forced change in the testing industry.

Now consider how the value in testing is distributed across process diagnostics, wafer sort, and final test. Some twenty years ago, the greater emphasis was placed upon final test, for it was here that the component had to pass muster. Wafer sort was only of secondary interest. Wafer-sort test-limits were guard-banded so pessimistically that many good parts in the marginal guard-band regions were thrown out in order to favor obtaining high yields at final test.

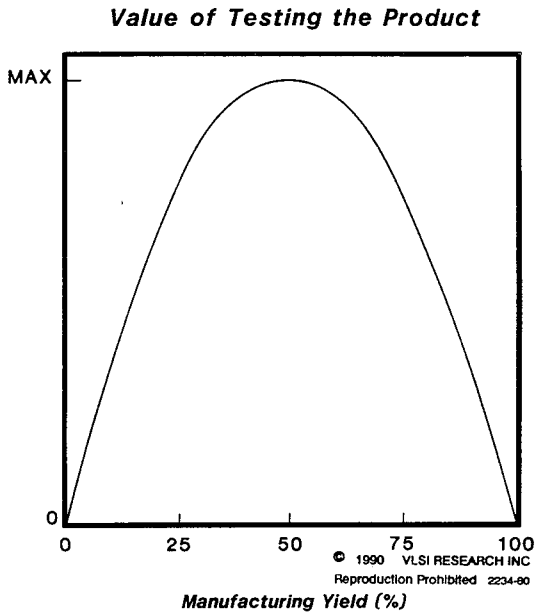


Source: Teradyne
2234-41

Figure 3.3.1.1-19

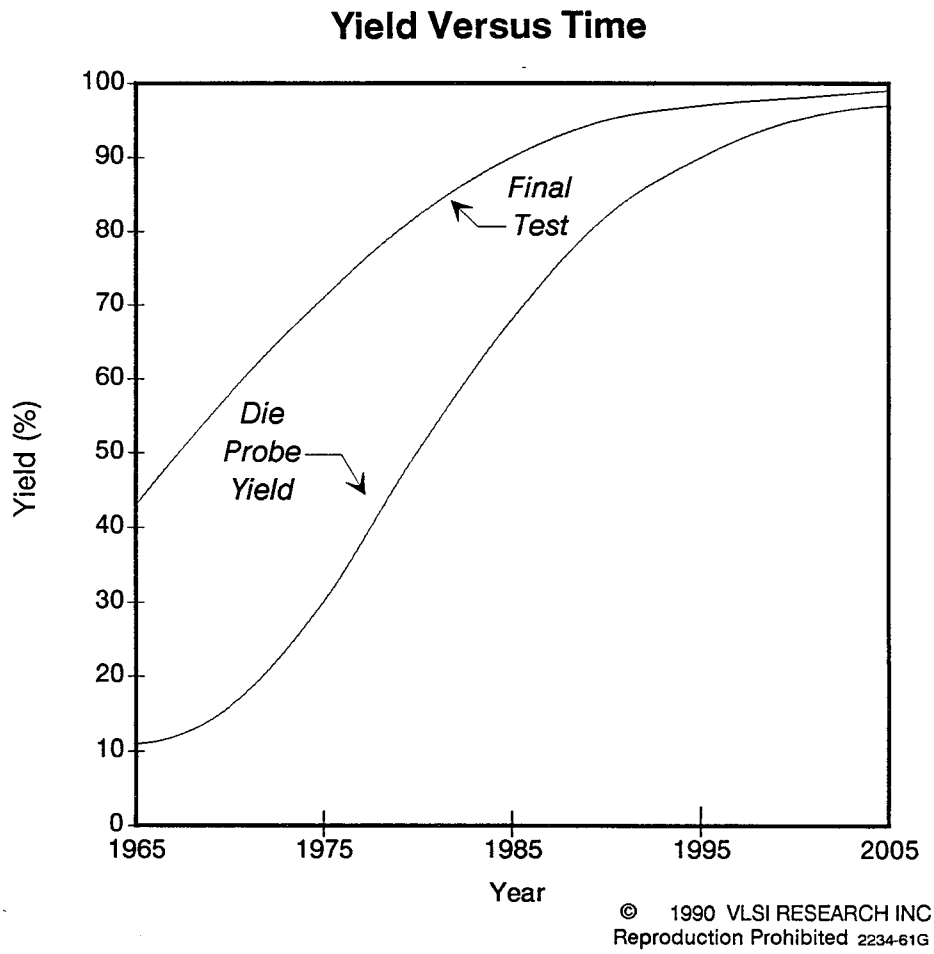
Configurability of the A510AL Advanced Linear Test System

Figure 3.3.1.1-20



As yields have improved over the years, the value in testing has shifted from final test back towards die-sort and process diagnostics. Process monitoring has become an acknowledged test point, too, for downloading test pressures and cost from test. It is an economic issue not a reliability issue. Thus, in today's environment, process diagnostics and test share about equal importance. The trend can be expected to continue as wafer sort becomes the major test points while final test becomes relegated purely to sampling procedures. This should force dramatic changes in test equipment. It is thus no coincidence that the major test and prober houses are focusing strongly on wafer probe. The pressure is building from their customers.

Figure 3.3.1.1-21



3.3.1.1.1 Market Segmentation of Logic ATS

- **Logic ATS can be segmented into eight classifications.**
- **The classifications are based on the maximum data I/O channels available and the maximum digital frequency attainable.**

Logic test systems are a single category of testers that is segregated by eight distinctive classes. These classes are based on a vector quantity that we have termed MDCR. The term is derived from Maximum Data Channel Rating.

Logic test systems, being digital in nature, tend to increase in complexity in a binary fashion, doubling with each new pair of bits added on the control bus. Consequently, pin capability tends to go up in doublets–or octaves. For example, they tend to increase from 16 to 32 to 64, and then to 128, 512, 1024 or 2048. Likewise, the frequency also tends to increase in octaves. But it increases from a decimal base rather than from a binary base. Frequency tends to increase from 5 MHz, to 10 MHz, and then to 20 MHz, 40 MHz, and so on to 80, 160 or 320. The new MDCR rating is therefore merely a recognition of these fundamental groupings that are provided within the equipment architecture itself.

The method formalized at VLSI Research is to use the maximum number of data I/O channels available, whether single or dual, together with the maximum digital frequency attainable, whether single or multiplexed. So as a case in point, a 20 MHz, 128 pin logic tester that is capable of 40 MHz in multiplex mode and 256 pin drivers in split I/O mode would be classed as a 256X40 tester.

Our analysis indicates that this will be a more fundamental measure of logic test equipment market boundaries than are other types of features available on the equipment. Moreover, by using broad enough categories, there is room left for the individual suppliers to be able to use specific feature sets as differentiating elements for their equipment without requiring an entire new definition with each piece of equipment.

Table 3.3.1.1.1-1 illustrates the effectiveness of this methodology with current types of testers. MDCR class 1 consists of those testers below 32X10; those in class 2 are below 64X20; those in class 3 below 128X40, etc. It is to be noted that while most tester types tend to occur at the corners of each class domain, there are still a few that are along the sides. So to accommodate these, a criteria has been developed to the effect that a tester will be included in any one class so long as either one of its vector elements exceeds the minimum class level for that class, while the other quantity equals at least one half of its class rating. This phraseology is codified in Table 3.3.1.1.1-2. As an example, a tester with a 128X40 MDCR rating would be in class 4 because it is at the class 4 corner. So too would be a tester with a 129X20 or one with 64X41 rating, since either of these exceeds one half of at least one of the vector quantities.

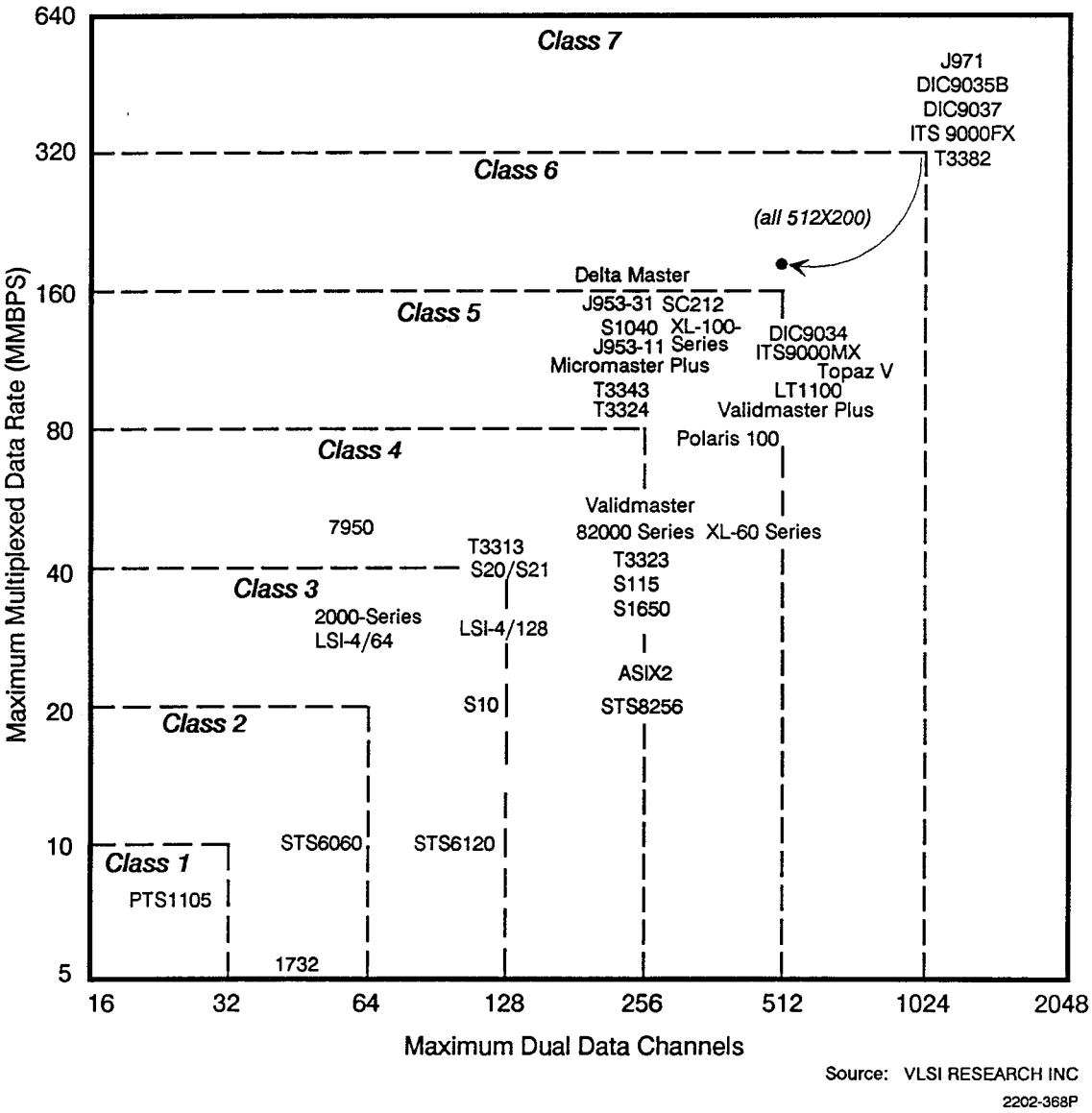


Figure 3.3.1.1.1-1

Graphical Portrayal of Maximum Data Channel Rating

(Testers are listed by model number only,
refer to other TABLES for manufacturers)

TABLE 3.3.1.1.1-2

DEFINITION OF MDCR CLASS FOR LOGIC TESTERS

The Maximum Data Channel Rate (MDCR) classification method represents a new classification scheme by VLSI Research Inc. for VLSI logic testers. This new class is a vector definition designed to better categorize logic testers markets by application. It is based upon the maximum multiplexed data channel rate of a particular system and its maximum channel size, when considering dual-channel pincards.

MDCR CLASS	*MDCR LOWER CORNER LIMIT* Master *(channel size x speed)*	*MINIMUM QUALIFYING CONFIGURATION (channel size x speed)*
0	-	-
1	16 x 5	17 x 3 or 8 x 6
2	32 x 10	33 x 5 or 16 x 11
3	64 x 20	65 x 10 or 32 x 21
4	128 x 40	129 x 20 or 64 x 41
5	256 x 80	257 x 40 or 128 x 81
6	512 x 160	513 x 80 or 256 x 161
7	1024 x 320	1025 x 160 or 512 x 321

A complete listing of all available logic test systems categorized by the MDCR class rating is given in Table 3.3.1.1.1-3.

This table also provides a price rating that can be used as a further crosscheck of the viability of this method of classification. Price rating is the average selling price of a system divided by the vector magnitude of its MDCR rating. vector magnitude is simply the root-mean-square value of the data channel rating (in pins) and the frequency (in MHz). Figure 3.3.1.1.1-4 provides a graphical correlation of the price index. Here it can be seen that there is a good degree of correlation between the vector magnitude of the MDCR and price.

Figure 3.3.1.1.1-5 places this rating on a more quantitative basis. In this figure, each machine is positioned by average selling price and by price index. It can be readily seen that there is in fact a loose correlation between MDCR and price. This occurs despite the various features available and it appears to be relatively independent of whether or not a tester-per-pin architecture is used.

Megatest	Impact-1	500	64	20	3	7.5
	Megaone	2600	256	80	5	9.7
	Polaris 50	2800	512	100	5	5.4
	Polaris 100	4300	512	200	6	7.8
Microcomponent Technology	2000-Series	350	64	33	3	3.1
	3100-Series	700	128	100	5	2.8
Minato	9200					
Pragmatic Test Systems	PTS 1010	75	24	8	1	2.4
	PTS 1100	40	24	8	1	1.3
	PTS 1105	100	24	8	1	3.7
Siemens	725					
	764		64	20	3	
	768					
Schlumberger ATE	S10	600	120	20	3	1.8
	S15	1170	256	40	4	2.6
	S20/S21	1200	120	40	3	3.8
	S50	4200	512	100	5	2.5
	S1650	1800	256	40	4	3.4
	S1040	2600	256	80	5	3.7
	ITS 9000MX	3200	512	120	5	5.3
	ITS 9000FX	4400	512	200	6	
Tektronix	LT1000	800	256	50	4	2.3
	LT1001	1200	264	100	5	3.5
	LT1002	1200	128	200	5	4.2
	LT1100	1000	512	100	5	1.5
	LT1101	2300	512	100	5	3.8
	LT1102	2300	256	200	5	6.2
	LT1201	650	64	100	4	3.8
	LT1202	650	64	200	4	2.1
Teradyne	J953-11	2300	256	80	5	5.2
	J953-21	3000	256	80	5	7.1
	J953-31	3600	256	100	5	8.4
	J971	6000	512	200	6	10.9
Valid Logic (IMS)	Logic Master XL-100 Series	800	448	100	5	0.9
	Logic Master XL-60 Series	570	448	60	5	0.7

Source: VLSI RESEARCH INC
2202-419P

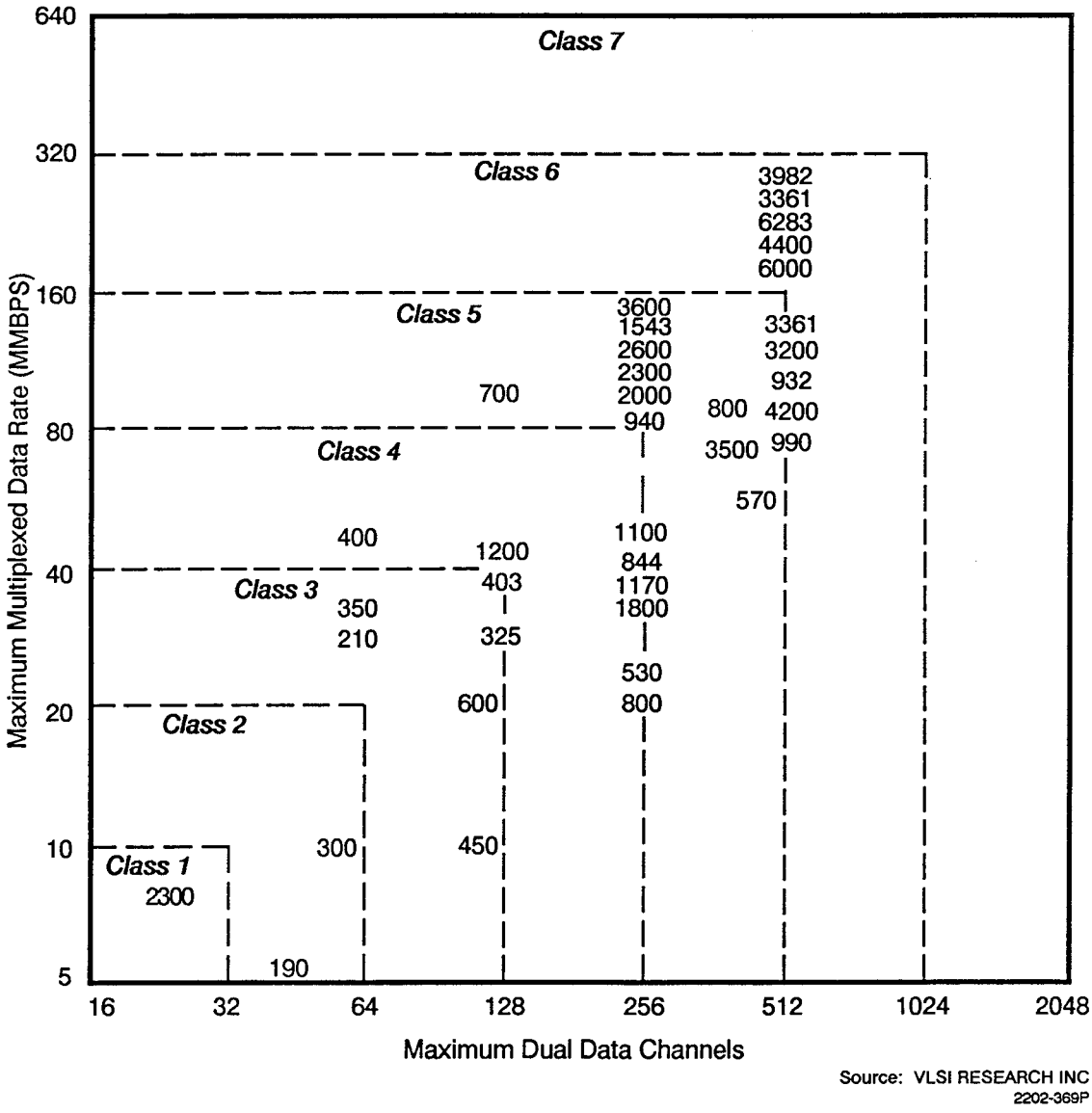


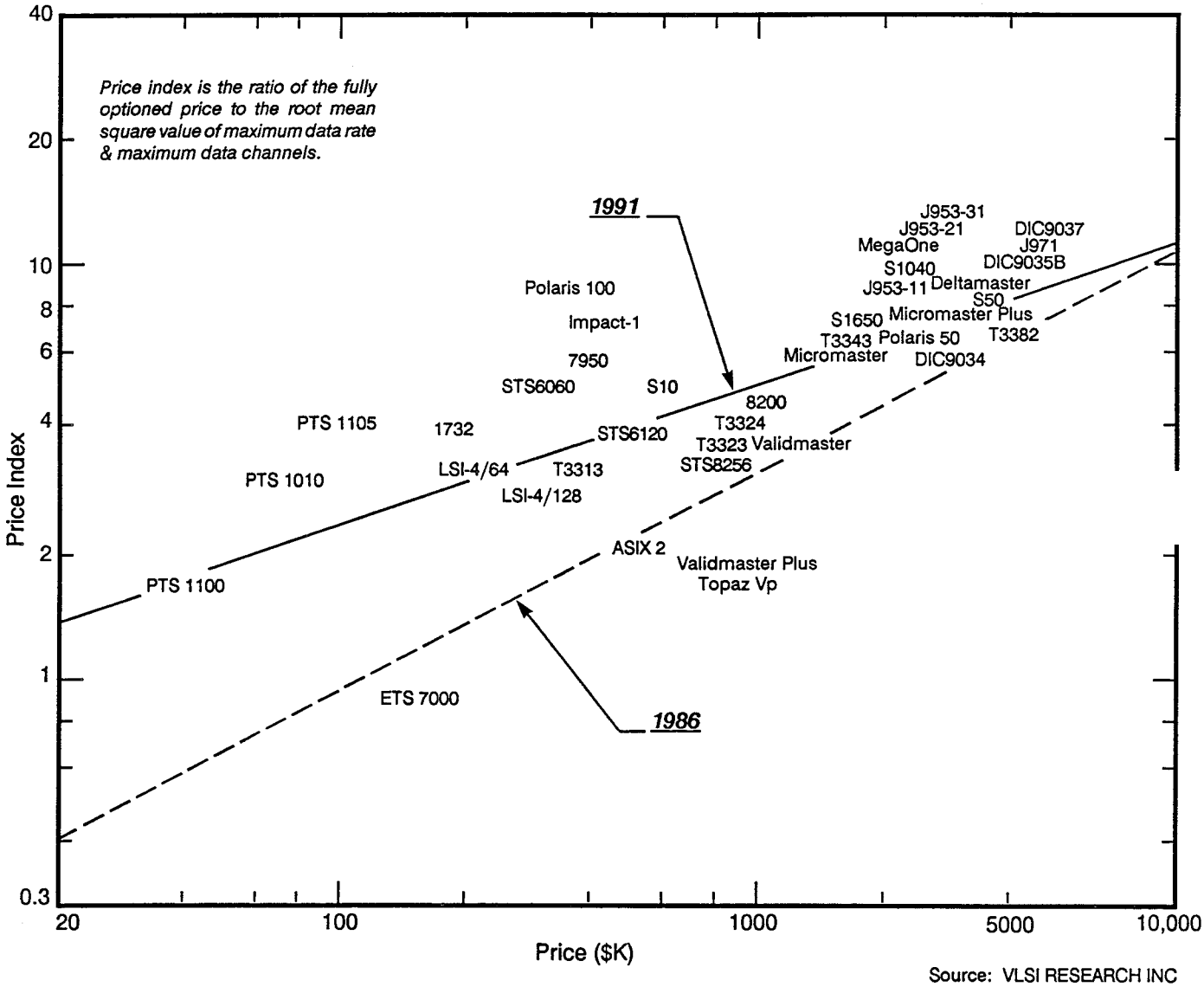
Figure 3.3.1.1.1-4

Correlation Between Price and MDCR

(Data Shown Inside the Chart is Average Selling Price in Thousands of Dollars for the Systems Shown in Figure 3.3.1.2.3-1)

Figure 3.3.1.1.1-5

WEIGHTED PRICE INDEX AS A FUNCTION OF PRICE FOR LOGIC TESTERS



Source: VLSI RESEARCH INC

2202-367P

3.3.1.1.2 Market Segmentation of Linear ATS

- **Linear ATS are segmented into traditional and mixed signal test markets.**
- **Mixed signal testers are further segmented by the primary application of the test system.**

VLSI Research categorizes linear testers into two sub-markets. The first consists of those traditional applications that need linear testers as they have always existed. The second group includes mixed signal testers. Mixed signal testers are further categorized by the primary application of the test system. The application categories include communications, converters, interface circuits, integrated signal processing, smart power and specialty mixed signal circuits. Table 3.3.1.1.2-1 depicts the type of devices that would be tested in each category.

The mixed signal tester market is classified by application for several reasons. Chief among these is the fact that each application brings unique testing problems. This can best be illustrated by looking at the functional blocks of some the more common advanced mixed signal devices. Figure 3.3.1.1.2-2 depicts the functional block of a typical analog dominant-technique circuit. In this case, a phase locked loop is shown. This is a fairly simple mixed signal device with a phase detector, low pass filter, high speed op amp and voltage controlled oscillator.

A more sophisticated interface device, a DASD file controller, is shown in Figure 3.3.1.1.2-3. Figure 3.3.1.1.2-4 depicts a video RAMDAC, a typical integrated signal processing circuit and Figure 3.3.1.1.2-5, an ISDN U-Interface communications device.

These figures indicate that mixed signal devices can become very complex. With this complexity, comes the need to control noise and to measure the timing delay between the digital and analog portion of the device. In order to address these problems for the diverse array of mixed signal devices available, many ATS vendors have begun providing specialized versions of their automatic test systems that are focused for a specific application. A good example of this is the Teradyne A500 family of testers. Teradyne offers the A510AL which is tailored for advanced linear devices, the A510SP which addresses smart power devices and the A520C which is used for testing consumer devices.

TABLE 3.3.1.1.2-1

MIXED SIGNAL TEST SEGMENTATION BY APPLICATION

- Communications
  - Telecommunications
  - Modems
  - CODECs
  - Universal Asynchronous Receiver/Transceiver(UART)
  - Intergrated Service Digital Network (ISDN)
- Converters
  - Analog-Digital
  - Digital-Analog
- Interfacing Circuits
  - Transceivers
  - Bus Interface
  - DASD Circuits
  - SCSI Circuits
- Integrated Signal Processing
  - Phase and Voice Array Signal
  - Digitial Signal Processing (DSP)
  - Video Palette
- Smart Power
- Specialty Mixed Signal Circuits
  - Automotive
  - Consumer
  - Industrial
  - Analog Dominant Techniques

Figure 3.3.1.1.2-2

Funtional Block of a Typical Analog Dominant Technique Circuit
(Phase Locked Loop shown)

MACRO CELLS

18001 - Phase Detector
12001,2 - Low Pass Filter
14002 - High Speed Op Amp
16001 - Volt. Controlled Oscillator

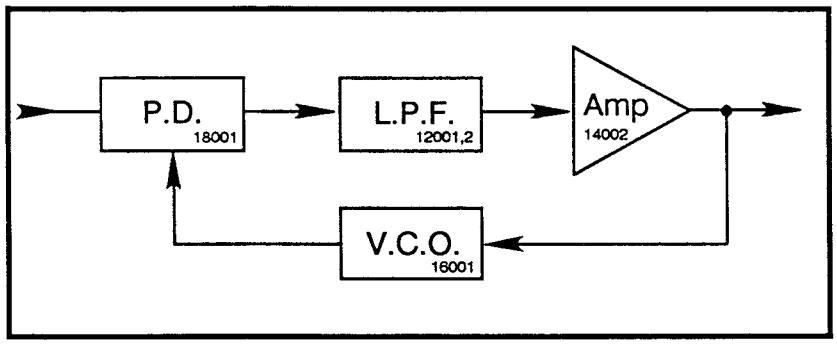


Figure 3.3.1.1.2-3

Functional Block of a Typical Interface Circuit
(DASD file controller shown)

MACRO CELLS

To be established.

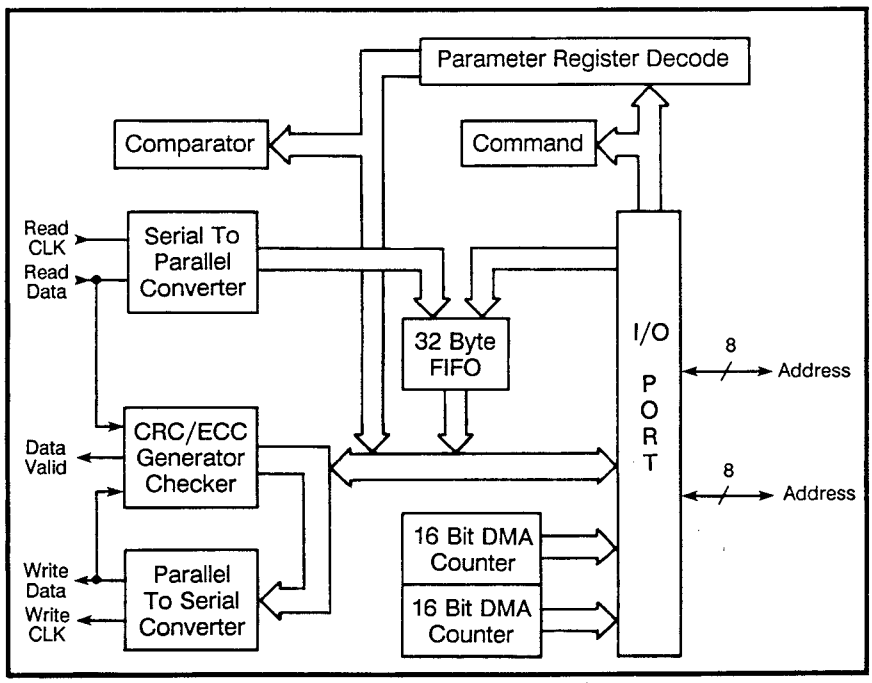


Figure 3.3.1.1.2-4

Functional Block of Typical Integrated Signal Processing Circuit
(Video Palette RAMDAC shown)

MACRO CELLS

17122 - D/A Converter
14001 - Op Amp
26012 - Address Latch

Address Multiplexer:
23010 - 8 Input Multiplexers
23005 - 2 Input Multiplexers

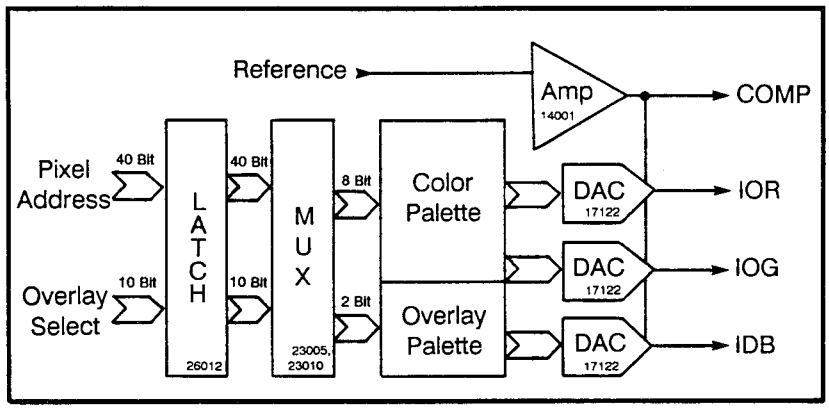
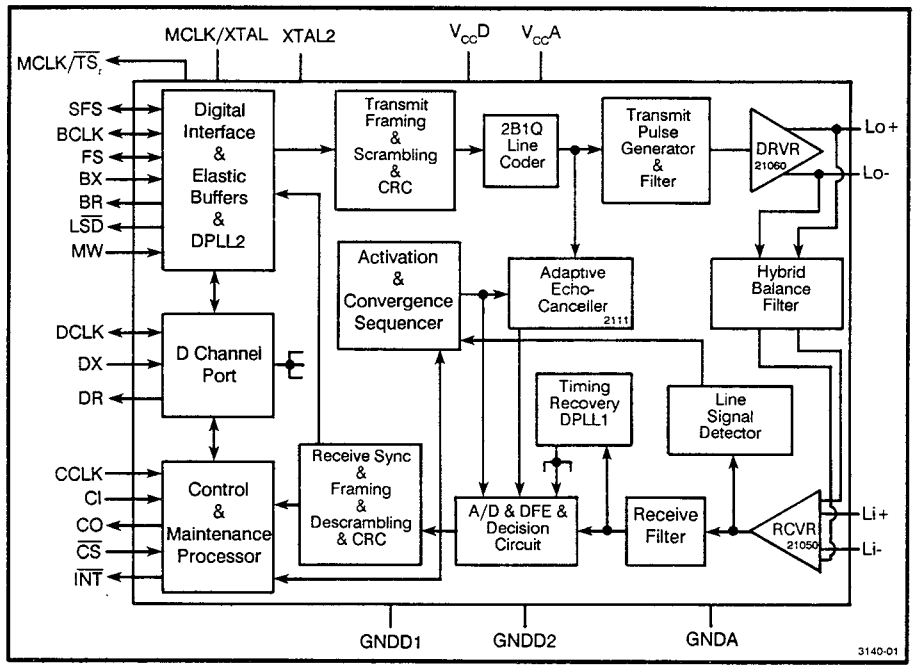


Figure 3.3.1.1.2-5

Functional Block of a Typical Communication Circuit
(ISDN U Interface shown)

MACRO CELLS

Hybrid Filter
Active Filter
Echo Cancellor
ADC
DAC
Driver
Receiver
DSP Processor
Digital Phase Locked Loop
Voltage Reference
Voltage Controlled Oscillator
Buffers
Multiplexer
de Multiplexer



3.3.1.2 Development of the Burn-In Industry

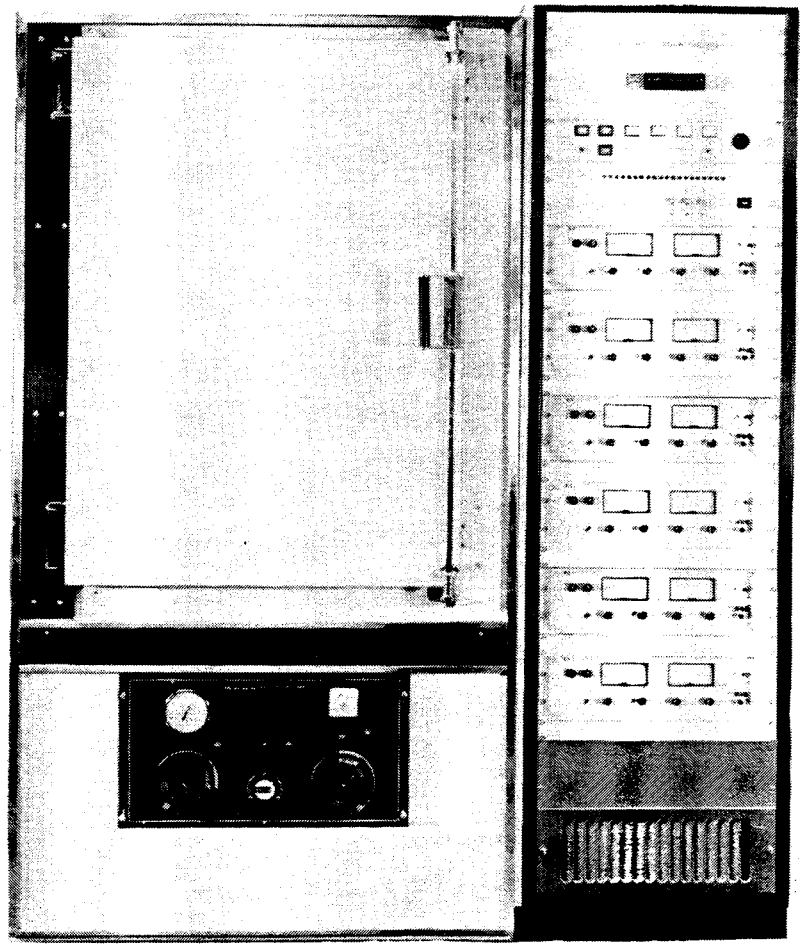
- **Burn-in is segmented into three categories: Static, dynamic and monitored.**
- **Burn-in continues to be driven by the evolution of DRAM technology.**

The burn-in industry began as a fragmented custom market. Prior to 1972, it existed mostly as an in-house engineering effort, as did much of the semiconductor captive equipment industry. Semiconductor manufacturers would purchase the burn-in ovens intact—usually from Blue M or Despatch—and would then build their own systems. Marin Controls and Aerotronics were two of the earliest commercial suppliers to exploit this captive market. A photo of the Marin Controls System 25 is shown in Figure 3.3.1.2-1. Neither of these two companies were successful. In 1981, Marin Controls was acquired and it was then shut down. Aerotronics became engaged in, and soon distracted by, burn-in of automotive parts. However, Aerotronics did survive in this field, and was acquired by General Signal.

Dynamic RAMs arrived on the burn-in scene in the early 1970's. These required dynamic burn-in as part-and-parcel of their manufacturing process. None of the suppliers who existed at the time could satisfy this new burn-in requirement. The most complicated systems of the time followed MIL-STD 883 ring-oscillator burn-in procedures. But RAMs did not fit easily into this burn-in category. So the Test Service Laboratories took on the task of RAM burn-in. Pacific Reliability Labs, DCA Reliability Labs, Continental Test Labs, Reliability Inc., Trio-Tech, and Microtest were some of the larger test service laboratories who grew up to service this market. Most of these subsequently began to market the equipment they had begun building for themselves. Reliability Inc., Microtest, and Trio-Tech are outgrowths from that industry. Trio-Tech and Reliability Inc. continue to supply both systems and services to this day. Microtest divested its service business, which is today known as Alpha-Test. Microtest was then acquired by EG&G wakefield.

Among the other early competitors, Aehr Test was a spin-out from Marin Controls in 1977. AMT is a 1979 spinout from Microtest. Loranger integrated vertically; first from being a socket manufacturer for burn-in boards to become a burn-in tray supplier. Then they moved into Systems. Micro Control is a Minnesota-based company which has its origins in Control Data Corporation. Wakefield is also an early supplier of burn-in trays that integrated upwards. E.J. Systems spunout from Wakefield.

The term 'burn-in' is usually meant to include only those types of accelerated test methods which induce failures by carefully arranged combinations of temperature, time and voltage. The term is not meant to include shelf life tests such as, for example, when semiconductor components are placed in a tray and merely baked in an oven. Nor does it include shock tests such as when the parts—again in a tray—are cycled through hot and cold chambers.



Ref: Marin Controls Company

2234-33

Figure 3.3.1.2-1

The Marin Controls System – An Early Static or Dynamic Burn–in System

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The primary purpose in performing burn-in is to stress-test the components in a manner that will force the weak, unreliable, units to fail prematurely, while not overstressing the normal components. Burn-in is an inexact science requiring careful preplanning. This is because all the components to be tested were functioning normally beforehand. Only a small portion should fail if the lot was good and the test was performed properly. Afterwards, all should continue to function except for the so-called 'weak sisters'. These will have failed. In order to ensure that this occurs and that the 'weak sisters' do fail, the test must be very carefully designed so as to act as a reliability sieve.

A principal objective in performing burn-in is to get around the excessive and sometimes exorbitant cost of downstream failures. The economics of these future failures has been descriptively categorized in the so-called 'rule-of-ten'. This is explained in Table 3.3.1.2-2. The essence of the rule

is that the cost to detect and repair an IC chip that has failed will increase ten times with each succeeding test point. A field failure will cost $500. but a component detected in burn-in or test at the factory's incoming point of component inspection will only cost 50 cents. Back in the semiconductor factory it can be detected for even less. These excessive costs are a powerful and overriding economic incentive to perform burn-in. It is an incentive both to the supplier and to the end user of integrated circuits.

TABLE 3.3.1.2-2

The Rule Of Ten

At Each Preceding Step in Electronic System Manufacturing and Maintenance, the Cost to Locate and Repair a Faulty Integrated Circuit will Decrease by Ten Times.

Point of Detection	*Approximate Cost*
Field Service Call	$500
Pre-Shipment System Test	$50
Subsystem Board Test	$5
Incoming Inspection	50¢
* *	*
During IC Manufacture	20-25¢

There are three categories of burn-in. They are:

- Static Burn-In
  - HTFB (High Temperature Forward Bias)
  - HTRB (High Temperature Reverse Bias)
- Dynamic Burn-In
- Monitored Burn-In

One of the types of defects that burn-in is designed to detect is that due to contamination. Contamination failures are oftentimes caused by the presence of unwanted sodium. This itself is usually due to faulty cleaning procedures during manufacturing. Sodium contamination can be detected by applying a reverse bias voltage for some fixed time period at some fixed temperature. The test conditions will not change during this period, so it is known as static burn-in. The Marin Controls system shown in Figure 3.3.1.2-1 was a static system.

There are two methods of static testing, one is called HTFB and the other HTRB. HTFB refers to High Temperature Forward Bias. This denotes the test of a device at high temperatures, while its semiconductor junctions are forward biased. Such systems are almost exclusively dedicated to the burn-in of diodes and optical devices.

HTRB refers to High Temperature Reverse Bias. In this case the semiconductor junctions are reversed biased. Failures that are caused by migration of ions in dissimilar metallic bonds will be accelerated by an HTRB test. HTRB systems are therefore used in the burn-in of all manners of discretes, bipolar integrated circuits, linear circuits, and MOS integrated circuits. Most static systems are HTRB.

Dynamic burn-in requires a slightly different procedure. The objective is to operate a component in a manner that simulates its actual performance when placed under temperature stress. To do this it is necessary to switch the input signals to the device off-and-on and to drive the inputs as is done in actual device operation. This type of burn-in is called 'dynamic' or sometimes 'functional' burn-in in order to differentiate it from 'static' burn-in. Now, the reader should be careful to differentiate what dynamic burn-in is not. For example, it is not a test of functional performance at temperature extremes. That type of test is still done at final test. In fact, dynamic testing is done at temperatures substantially

above those specified as worst-case operating limits. For example, most commercial parts have high temperature limit specifications of +70 °C (+158 °F). But these parts are often dynamically burned in at 150 °C to 200 °C (302 °F to 392 °F).

Moreover, dynamic test is not an actual 'test' in the strictest sense of the word. Diagnostics are not being performed on the device during the time that dynamic burn-in is occurring.

Dynamic burn-in systems are used exclusively with digital components. Most are generally limited to RAM or Microprocessor devices. There are four primary components to a dynamic system. These are: The oven itself, the D.C. power supplies needed to supply the device-under-test (DUT), some driver circuitry capable of simulating the input of the device, and some kind of control circuitry.

The EG&G Titan system (See Figure 3.3.1.2-3) represents one type of burn-in system. This particular system can be made to perform in either a static or a dynamic mode. This system uses a popular 'feed thru' mechanism that keeps the electronic driving circuits at room temperature while the burn-in boards or 'trays'—as they are sometimes called—are kept inside the oven. Figure 3.3.1.2-4 depicts the scheme.

The oven system contains a stainless steel tray-frame assembly with precision alignment to assure mating when the tray is inserted. Rails are used to guide the tray into place and to provide proper alignment. The backwall insulation is thermally sealed with an inner and outer silicon rubber gasket and about 3.5 inches of glass wool material. Consequently, heat loss is at a minimum and the back wall is sealed for inert gas atmosphere.

A feedthru hole exists in the backwall. An extender card is inserted in each feedthru slot from the inside of the oven. This card consists of a pin connector soldered to a PC board. the extender card connector is secured to the inner wall of the backplane with two screws. All stimulus to the tray is then provided from outside the oven through the extender card.

A somewhat different system is provided by Kineticon, a Scottish firm. Its burn-in system is shown in Figure 3.3.1.2-5 while a photo of its universal burn-in tray, and a drawing of its carriage mechanism is shown in Figure 3.3.1.2-6.

The key feature of the Kineticon system is the unique design of the Kineticon burn-in board. The figure shows that the device sockets are located at one end of the burn-in board, while the test and control logic is clustered at the other end. An insulated wedge made of a three inch thick silicon foam separates the device sockets from the logic. This wedge provides a comprehensive seal in the oven wall when the carriage mechanism is activated, placing the devices under test into the elevated temperature region while leaving the test and control logic in the ambient temperature zone.

The actual board is housed in a molded plastic frame, and the logic circuitry at the front end of the board is protected by a molded cover integrated into a carrying handle.

Monitored burn-in is the most recent form of burn-in that has emerged. Monitored burn-in differs from dynamic burn-in on one significant point: the output of the integrated circuit is being monitored or tested and diagnostics are being performed during the actual burn-in period. In this case, the objective is purely economical and generally only of use to the semiconductor manufacturer, not to the end user. It happens that the required methods for electrically testing the device have grown uneconomically long. This is particularly true for memory testing.

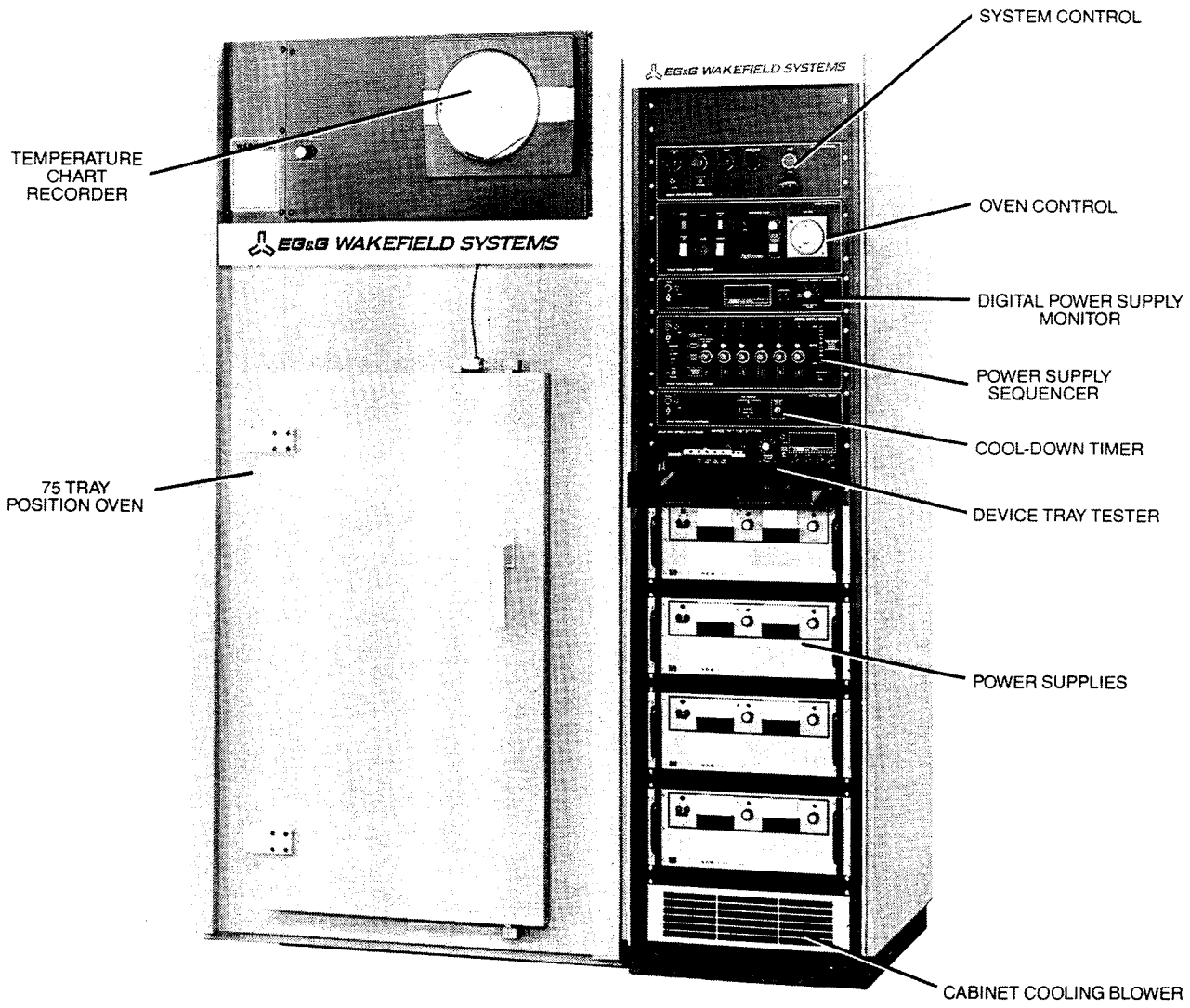
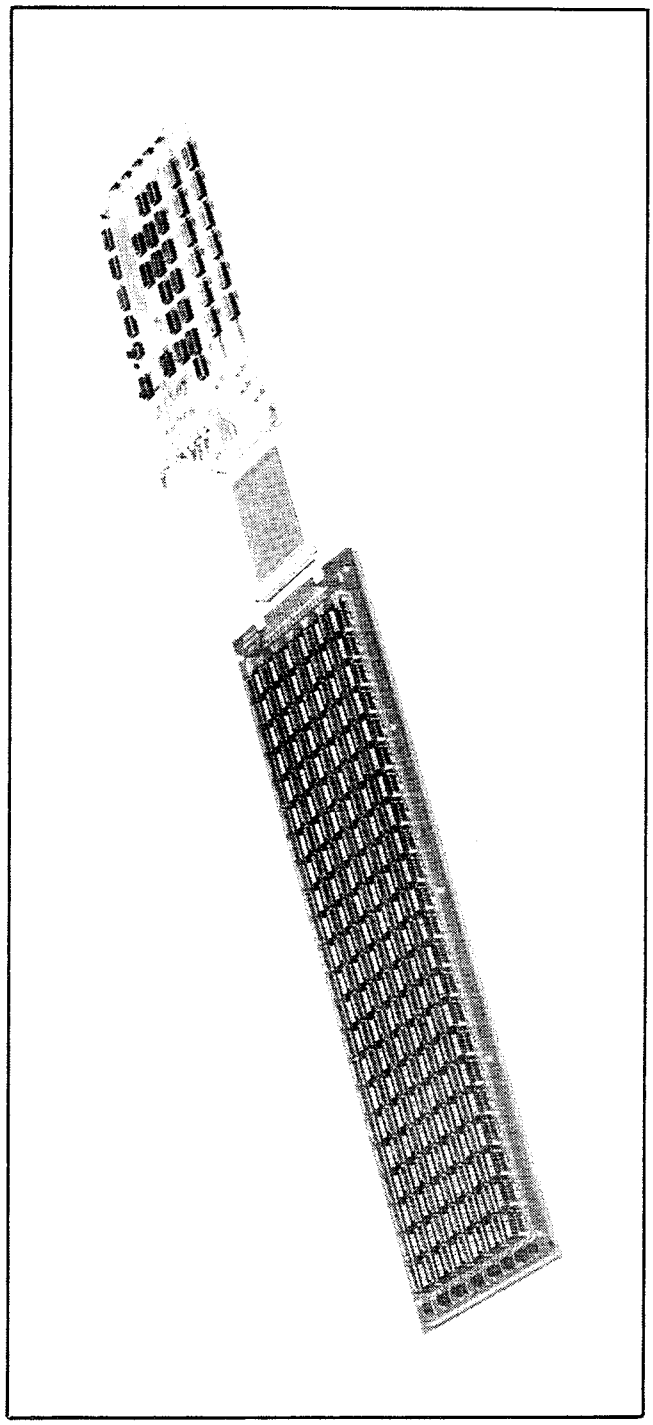


Figure 3.3.1.2-3

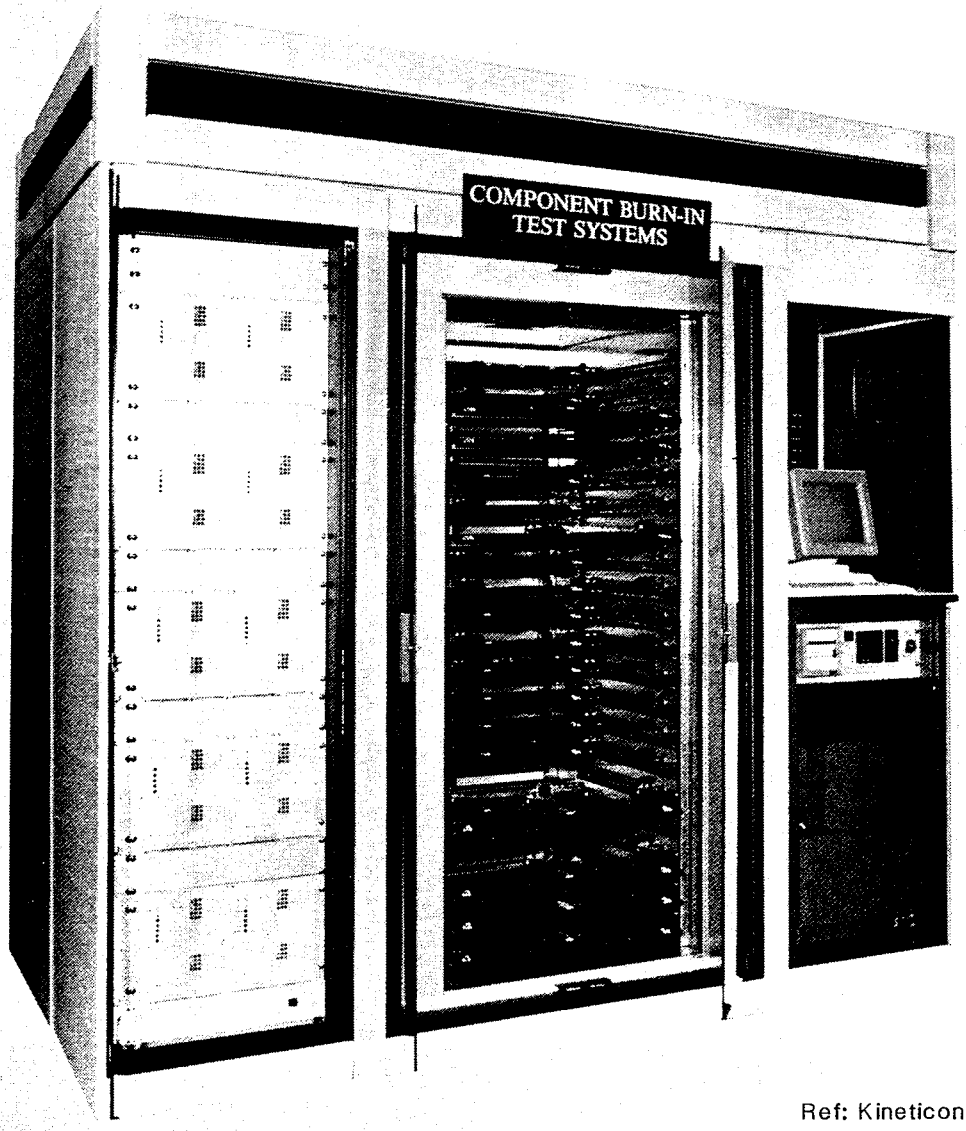
The EG&G Model 500A-75



Ref: EG&G 2234-50

Figure 3.3.1.2-4

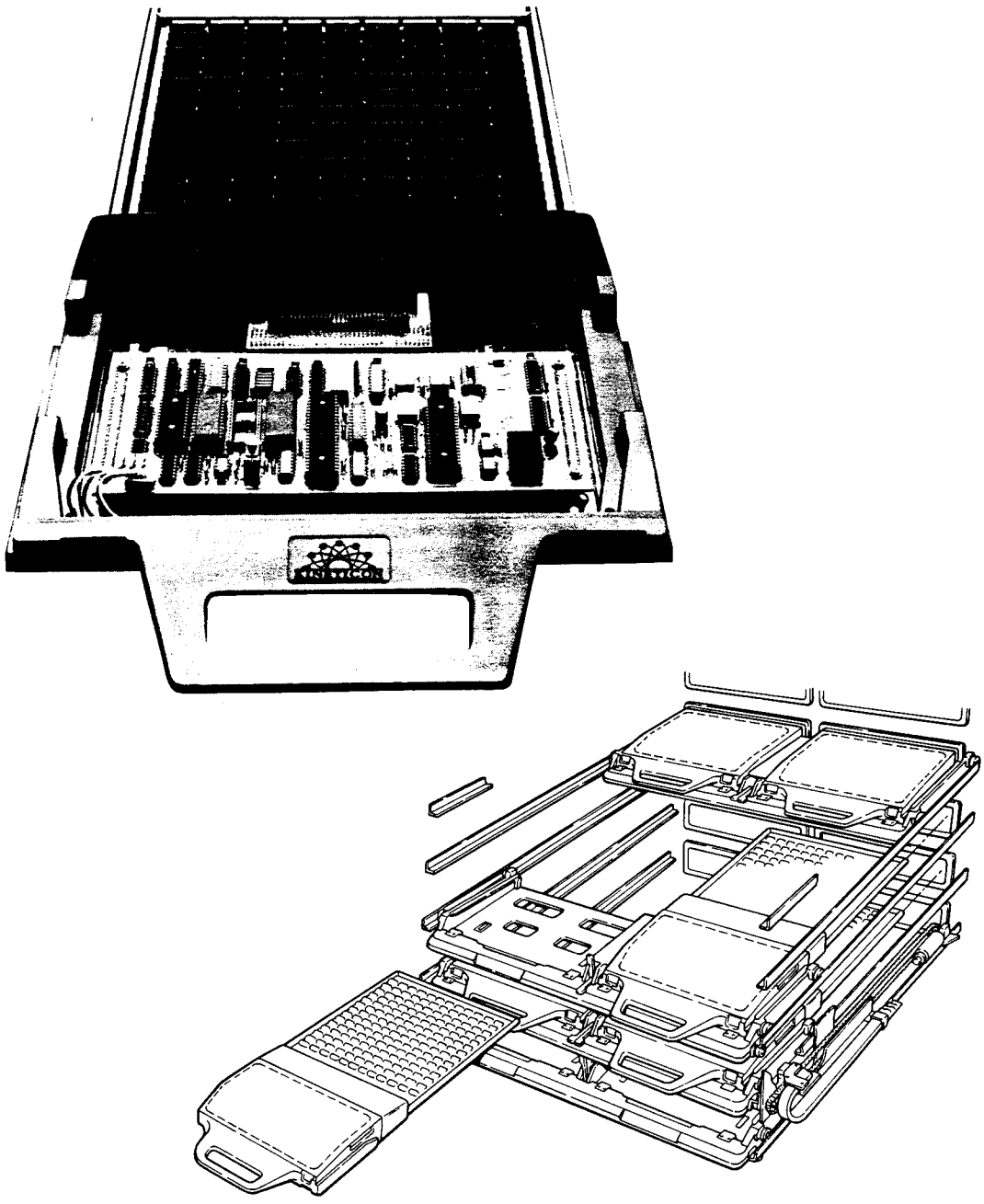
Burn-in Tray, Extender Card and Exerciser Card



Ref: Kineticon
2234-47

Figure 3.3.1.2-5

The Kineticon Dynamic Burn-in System



Ref: Kineticon
2234-48

Figure 3.3.1.2-6

The Kineticon Burn-in Board with its Fixturing Mechanism

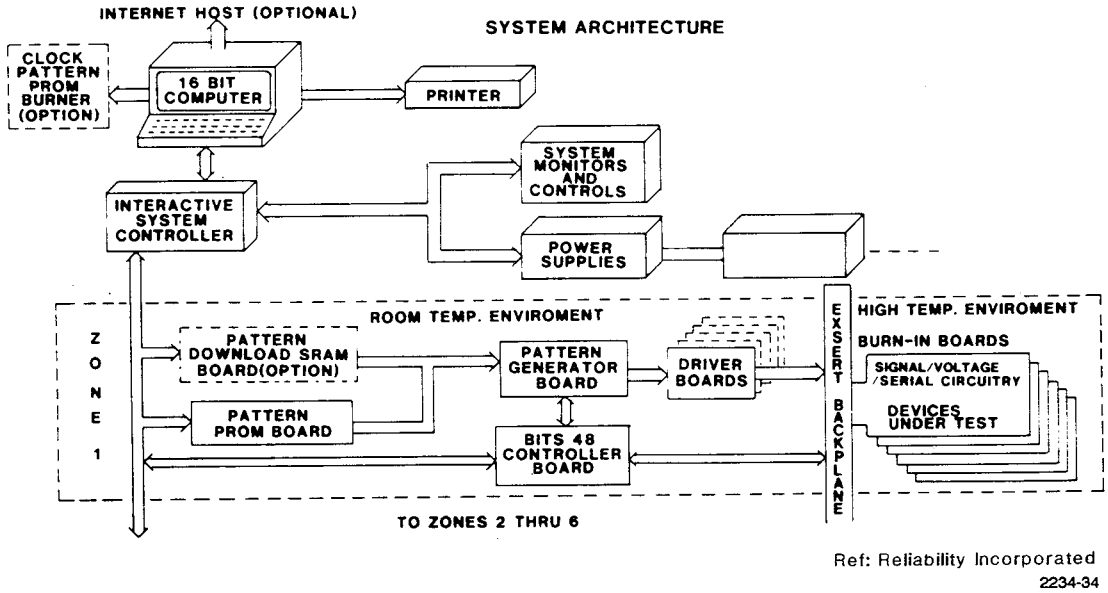


Figure 3.3.1.2-7

Block Diagram of a Monitored System

Excessive test time on such expensive machines cannot generally be passed on to the buyer. But the bulk of these tests can be done by the dynamic burn-in equipment already in the burn-in ovens, and at only a fraction of the regular test cost.

Physically, the system appears the same as any other system. Electronically, it has additional sensing circuitry. Figure 3.3.1.2-7 depicts the block diagram of a typical monitored burn-in system.

The trend to monitored burn-in can be expected to accelerate along with the trend towards larger memory. One and four megabit DRAM's have been in production for several years. Sixteen megabit DRAMs will follow in 1991. The trend in memories is clearly continuing towards ever-larger complexities with a 64 MB DRAM in sight. This trend has brought enormous pressure to bear upon reducing test-time-demand. As an example, the one megabit DRAM has a minimum cycle time of 600 nanoseconds. A Galpat type of memory test on this device would require 1333 hours. This is more than eight full weeks just to test one device. Moreover, a more conventional memory test known as a three-halves power test would require 1.3 hours. The cost to perform either of these tests would far exceed the going price of the device itself.

In order to reduce such associated test costs, manufacturers are turning to functional testing while the memories are being burned-in. Two things are thereby accomplished. First, the time to burn-in the device has already been taken up, so the time taken to test comes virtually free of cost. Second, the unit is also already at its high temperature limit, so high temperature handlers will not be needed at final test.

The latest strategies for monitored burn-in call for a short burn-in time between 4 to 8 hours as contrasted with the more usual 24, 48 or 168 hour periods. This short burn-in is then followed by a functional test. If the

units pass the test, burn-in can be stopped. But if they fail a critical lower quality limit, the burn-in is continued for a while longer and then rechecked. This test sequence is repeated several times until a designated quality level has been reached. Often, the burn-in can be stopped after one cycle if the lot quality exceeds historical standards. These standards are determined by having tracked previous lots. Consider the following data taken at Motorola in 1987:

Total Number of Devices on Burn-In	*Burn-In Duration (hours)*	*Cumulative Failures*	*Failures Per Cycle*
2400	6	20	20
2380	12	25	5
2375	18	28	3
2372	25	30	2
2370	30	31	1
2369	36	33	2
2367	42	34	1
2366	54	38	4

This data was obtained on 64K DRAM's stressed at 8 volts while at a 125 °C dynamic burn-in temperature. Fully 53% of all cumulative failures occurred within the first six hours. And after only 12 hours, some 66% of the failures had been detected. Some 74% accrued within 18 hours.

The monitored burn-in cycle has two beneficial effects. The first is that good devices will not be needlessly damaged by excessively long burn-in times. This ensures high-quality while improving yields. Second, far less burn-in equipment and cost will be needed to equip one production line. In fact, the total number of systems needed for monitored burn-in is only about 30% of that needed for dynamic burn-in. There will be additional cost savings in lower floorspace and labor requirements.

Burn-in at high temperatures often requires that the devices be contained in an inert atmosphere such as nitrogen. Moreover, the devices are consuming power and thereby getting hotter, while the controlled atmosphere will not always carry away the excess heat. These limitations have caused some manufacturers to consider liquid burn-in systems.

In liquid burn-in systems, the devices are immersed in an inert liquid rather than in air. It is usually a freon such as FC-40. Power is applied to the device while in the liquid.

Liquid burn-in is especially applicable when burning-in power devices that may have a high junction-to-case thermal resistance. If a device generates more than about five watts total power and has a junction-to-case thermal resistance of more than 10 ° C/W, or if a device has a junction-to-case thermal resistance of 25 ° C/W and generates two watts, liquid burn-in can be considered.

In addition to excellent heat transfer, which minimizes the temperature differential between the case and liquid and prevents burn-out, other advantages of liquid burn-in include:

- excellent temperature control and stability.
- no oxidation.
- space savings, and
- access to individual fixtures without interrupting burn-in of other fixtures.

Temperature stability in liquid burn-in systems is better than it is in air systems. With proper agitation and mixing (50 gallons per minute of stirring for 50 gallons of liquid), the temperature gradient throughout a system will be less than ± 0.5 ° C even with full power applied (5,000 W). Burn-in of multiple devices can therefore be accommodated with no hot spots.

While these advantages appear to be cogent, liquid burn-in has yet to make an appreciable impact in burn-in, and has had only a few sales.

FTS Systems in Stone Ridge, NY manufactures a liquid burn-in system. Figure 3.3.1.2-8 depicts its architecture.

ɔn Circuitry To assure proper burn-in and prevent overheating, standard, built-in safety circuits disable the heater and can be used to cut off power to the boards if tripped by any of the following fail safes:

- **Low liquid level** – protects against unsubmerged devices.
- **Low flow** – warns of insufficient fluid flow which could reduce the heat removal rate.
- **Overtemperature** – protects devices against fluid temperature rising above a set point.
- **"Home" lifter position** – prevents power from being applied when lifter is in up position.

2

Filtering Filtering removes contaminants such as water, acids, corrosives, board residues and particulates, to ensure clean operating fluid. A large-particulate screen on the pump inlet screens out gross particles. A 10 micron charcoal/desiccant blend filter cartridge continuously filters 5 to 10 percent of the liquid passing through the heat exchanger.

All filters can be serviced while the system is operating, allowing the burn-in run to continue undisturbed.

3

Vapor Recovery System

The vapor recovery system – operates continuously so you can access fixtures at any time. At the end of a burn-in run, the pneumatic cylinder lifts the fixture into the freeboard area, where boards drain and dry before removal. The vapor recovery system removes all vapors and condenses them into fluid, which is then pumped back into the bath. The boards are dried and ready for removal in minutes. Fluid loss usually associated with drag out or vapor losses is minimized.

4

Water Removal A water separator in the liquid return line prevents condensate from returning to the bath. A vapor scrubber cartridge is incorporated into the vapor recovery system to trap any corrosive condensate present in the system.

5

Fixturing Fixturing is available in two standard configurations

Fixture Type 1

The first configuration is used by manufacturers who need to burn in small lots of varying types of devices. The fixturing provides up to 80 positions for 4.5"W (11.43 cm) burn-in boards. Up to 13 different voltages may be applied to each burn-in board

Fixture Type 2

The second configuration is used by manufacturers with larger lots. The fixture allows up to 24 boards to be mounted on 1.375" (3.43 cm) centers. The burn-in board is 16"W x 10"H (43.64 cm x 25.4 cm). Each burn in board can handle up to 25 individual voltages and 60 monitoring points.

Both fixturing methods allow zoning of power for separate and unique burn-in runs.

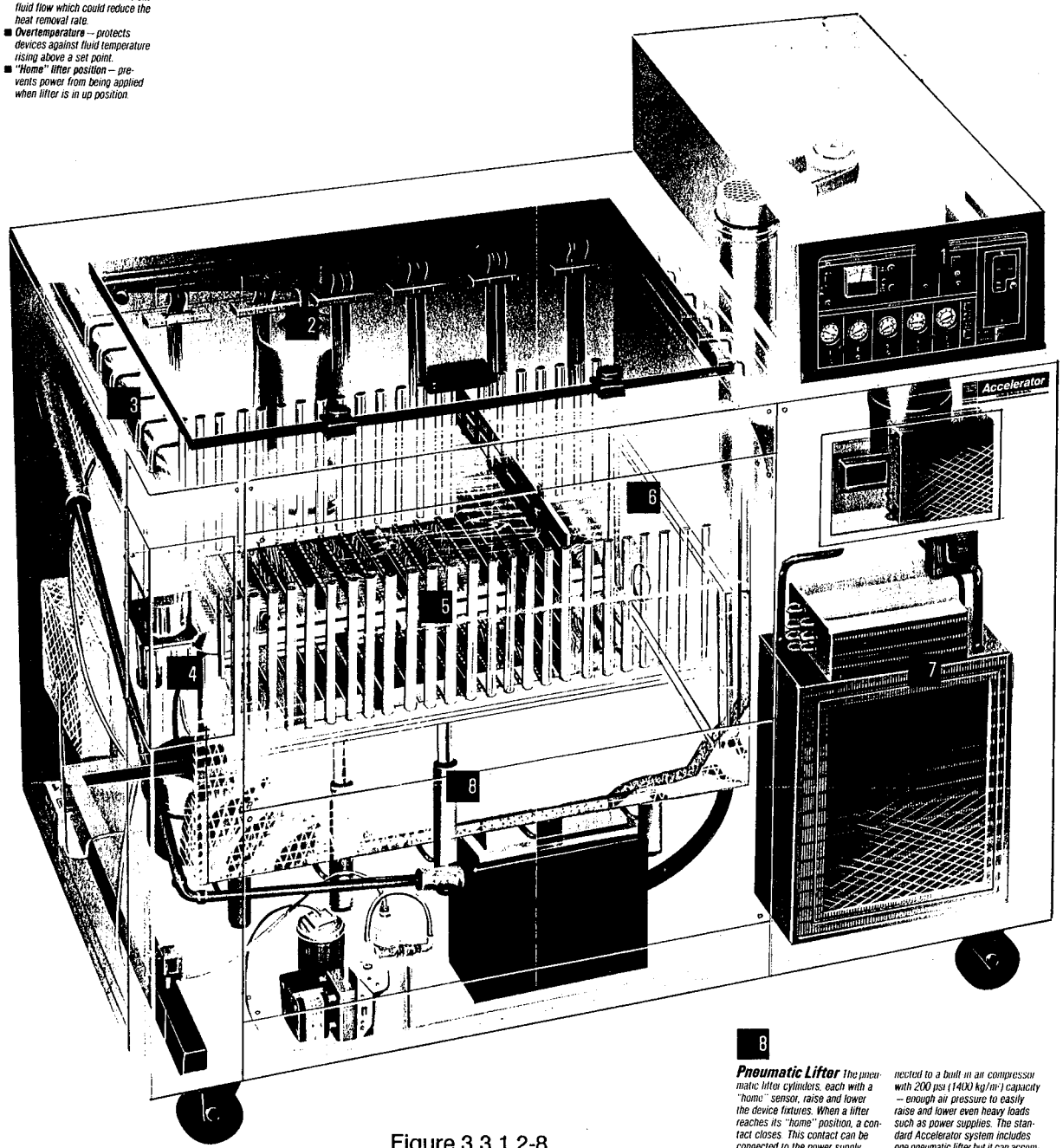


Figure 3.3.1.2-8

The FTS Liquid Burn-in System

6

Agitation A high-volume (50 GPM/185 LPM) pump and suction port system agitates the fluid, attaining a velocity of more than 70 feet/minute (22 meters/minute) for precise temperature control and device stability.

The pump speed accommodates dielectric fluids with different viscosities, allowing efficient operation at any temperature. Bath porting amplifies fluid flow to create a complete mixing action that prevents temperature stratification.

7

Heat Removal Dielectric fluids can remove more heat per unit area than air or nitrogen. By combining forced convection, subcooling and boiling, Accelerator systems can control watt densities over 125 watts/sq. in. (19.4 watts/sq cm.)

The standard Accelerator includes an air-cooled mechanical refrigeration system capable of removing up to 7500 watts of power at +125°C. The Accelerator Jr can remove 2000 watts of power at +125°C.

Self-contained mechanical refrigeration allows cooling at or below ambient temperature and requires no expendable coolants. However, room temperature must be maintained at or near 72°F (22°C) for maximum performance. Since the Accelerator generates heat into the environment, auxiliary room cooling may be necessary.

Heat removal options:

Water-cooled refrigeration

A mechanical compressor, cooled by circulating water, compresses Freon and expands it in the heat exchanger. Less heat is exhausted into the room and the bath can be cooled to below room temperature. Plumbing is required, however, and the expense of cooling water must be taken into account.

Water-cooled heat exchanger

Tap water (2-8 GPM/7.6-30 LPM) or recirculating water circulates through the heat exchanger.

As in water-cooled refrigeration, heat isn't exhausted into the room. The water-cooled heat exchanger allows higher heat removal than is possible with mechanical refrigeration – up to 12,000 watts. Heat removal is tied to water temperature and flow – no heat removal is possible at or below the water temperature. Also, plumbing is necessary and the expense of cooling water must be considered.

Heat up/Cool down times (without a load):

	25°C / 125°C	125°C / 25°C
Mechanical refrigeration	3 hrs	1.5 hrs
Water cooled heat exchanger	3 hrs	1 hr

8

Pneumatic Lifter The pneumatic lifter cylinders, each with a "home" sensor, raise and lower the device fixtures. When a lifter reaches its "home" position, a contact closes. This contact can be connected to the power supply system to ensure that boards are powered up only when the cylinder is in the proper position.

Each pneumatic cylinder is connected to a built-in air compressor with 200 psi (1400 kg/m²) capacity – enough air pressure to easily raise and lower even heavy loads such as power supplies. The standard Accelerator system includes one pneumatic lifter but it can accommodate up to five pneumatic lifters – letting you process up to five individual burn-in runs in the same system.

Ref: FTS
2234-35

3.3.1.3 Development of the Design Diagnostic Industry

- **The design diagnostic industry is subsegmented into circuit probers and modification tools.**
- **Circuit probers include E-beam and laser beam design diagnostic system.**
- **Modification tools include FIB systems.**

Design diagnostic systems is subsegmented into two categories. These are:

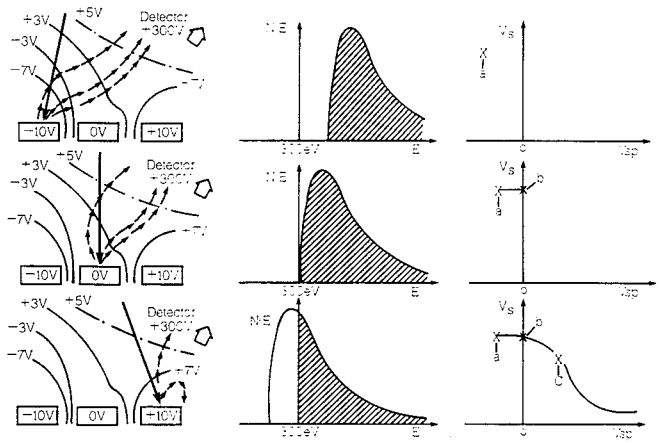
- Circuit Probers
- Modification Tools

Circuit Probers are primarily E-beam or laser beam based systems used for design diagnostics. This type of equipment is used primarily for failure analysis in the R&D environment using a non-contact method. Brief drawings of Circuit Probers are shown in Figure 3.3.1.3-1.

Part of the technology used in E-beam design diagnostic systems was developed in the mid-1960's by Graham Plows and William Nixon in the United Kingdom. It was not until the mid-seventies that IBM and Siemens had perfected the technology into the first E-beam design diagnostic system. Siemens developed the technology for captive use. Lintech and Integrated Circuit Testing (ICT) were the first companies to develop a commercial system. The Lintech system became available in 1980. Hitachi entered the market during 1983. Other companies to introduce system are Applied Beam Technology, Cambridge and Schlumberger. Mitsui-Comtek has also entered the market with a laser-based design diagnostic system, developed by Dataprobe.

An E-beam circuit prober consists of an E-beam system and a scanning electron microscope (SEM). The approach used is much like that used in the scanning electron microscope. Useful results depend upon the fact that data is stored as stored electrical charges. The scanning electron beam will interact with these stored charges and be able to 'see' different light or dark spots on a chip based upon the charge available. The scanned area will be light or dark depending upon whether a 'zero' or a 'one' has been stored.

E-beam circuit probers have been previously unsuccessful because of two reasons: Firstly, they were too slow to be of practical use in production applications. Secondly, the test results obtained were visual rather than electrical. These were not amenable to the precise measurements needed due to the numerous changing lights—at least not without a means of comparison against some known standard. The primary advantage E-beam systems offer is that they allow diagnostic testing of a subsystem within a large silicon based system. This has important benefits for researchers who are developing VLSI devices, for it allows detection of design defects, structural defects, and operational malfunctions of these isolated portions. The defects may lie buried unless the



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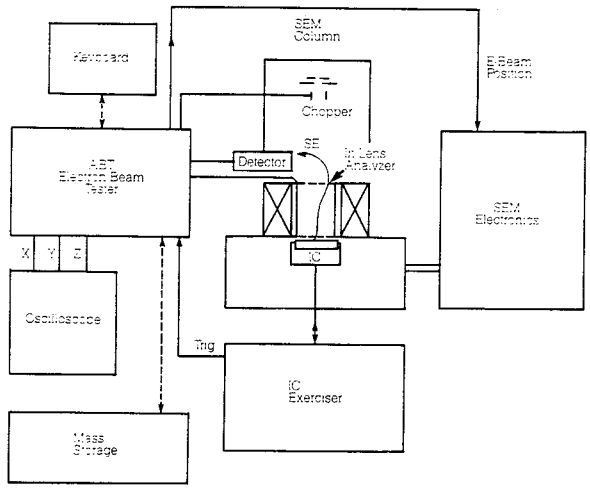
Origin of Voltage Contrast



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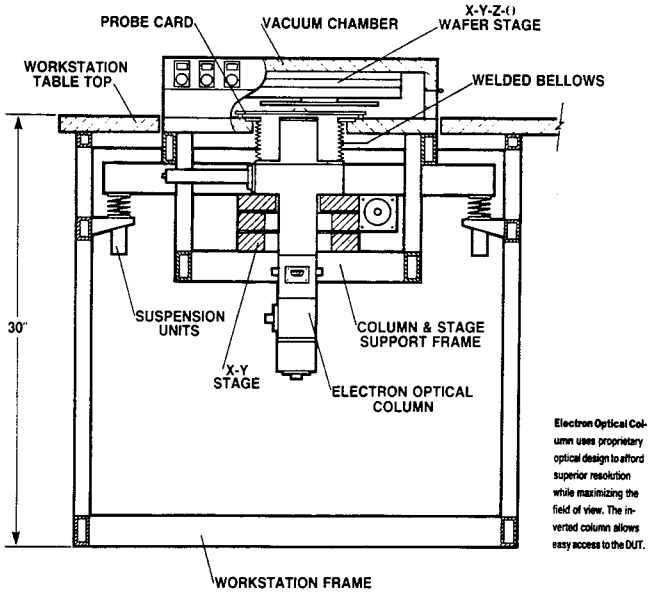
ABT/ISI Design Diagnostic System



Ref: Sentry

2234-46

Sentry IDS 5000

Figure 3.3.1.3-1

TYPICAL DESIGN DIAGNOSTIC SYSTEMS

entire system can be tested. Consequently, E-beam circuit probers have developed into an analytical tool for R&D purposes.

The non-contact probe on the E-beam allows the system to test devices as geometries continue to shrink. Manual contact probers generally cannot be used below 1.0-micron because the probe point is too large for interconnection and difficulties arise even at 1.0-micron.

The scanning electron microscope allows a design engineer to actually see the logic flow within a functioning integrated circuit. The design engineer can see where a fault originates and subsequent failures as they continue through the device. Additionally E-beam as well as laser-beam based systems compare information from a known good device and superimpose it on a questionable device searching for variations and thus possible failures.

Laser-beam circuit probers are used much like the E-beam systems except they employ a laser. One advantage that laser beam systems offer is that they do not require that diagnostics be conducted in a vacuum environment. Also laser beam systems do not require a stub to penetrate a passivation layer, as does an E-beam system. The major disadvantage with laser beam probers is that they are limited to non metalized areas where the laster beam will not reflect off the metalization layer.

Mitsui's laser design verification system may offer a more viable solution. It has no potential for damaging the circuit. It is not necessary to remove the passivation layer. It's main limitation is that it works primarily on CMOS. This is not too significant a limitation, however, since most available ASIC devices are CMOS.

Laser design diagnostics work by positioning a laser beam on the source or drain of a transistor. The photoelectric interaction of the transistor is then measured. Actual logic states are shown on a video scan.

Both methods offer the potential for getting into the circuit in a guided probe fashion. This increases the number of available nodes that an output can be obtained at. Thus, E-beam and laser design diagnostic systems are looked upon as powerful tools. Because of this, both testing and probing have undergone some fundamental changes, as these methods have reached the R&D environments.

Modification tools are primarily made up of Focused Ion Beam (FIB) systems. FIB modification tools were introduced with a lot of fanfare in the early eighties—after which they almost disappeared. Like its acronym implies, it was another technology that over-promised and under-delivered.

Nevertheless, the time eventually came for the technology. A lot of development has gone into FIB's since the early eighties. FIB modification tools are becoming accepted as an important IC development tool. Especially by semiconductor manufacturers who are creating proprietary products. The benefits of FIB modification tools are realized through the system's ability to cut traces, to drill through oxides and to selectively deposit tungsten for patching traces together. (See Figure 3.3.1.3-2). In essence, the system's focused ion beam allows it to perform microsurgery on a chip at geometries that are well below one micron. The system starts by selectively etching films. A beam cuts traces and drills contact windows. It then introduces a tungsten based goes and uses beam energy to selectively deposit tungsten patch wires on the circuit. It can also be used for making selective cross sections of a die or for evaluating crystal damage.

This makes FIB's absolutely essential to IC designer since they reduce costly mask redos during IC development. This capabil-

ity saves the semiconductor manufacturers both resources and development time. This leads to quick turnaround times and reduces redesigns cost which gives the semiconductor manufacturers a competitive edge in the market place. In fact, one user claims that FIB's save 13 to 16 weeks of development time.

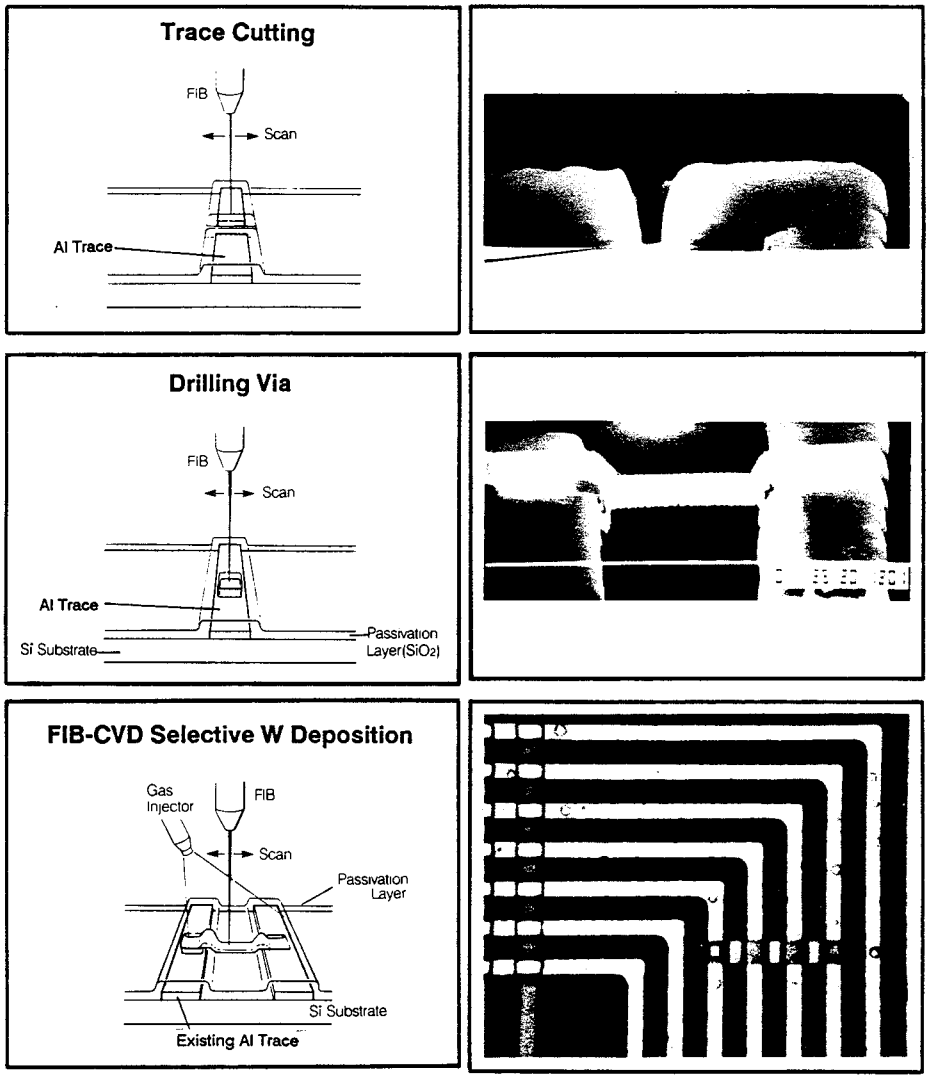


Figure 3.3.1.3-2

Capabilities of FIB Modification Tools