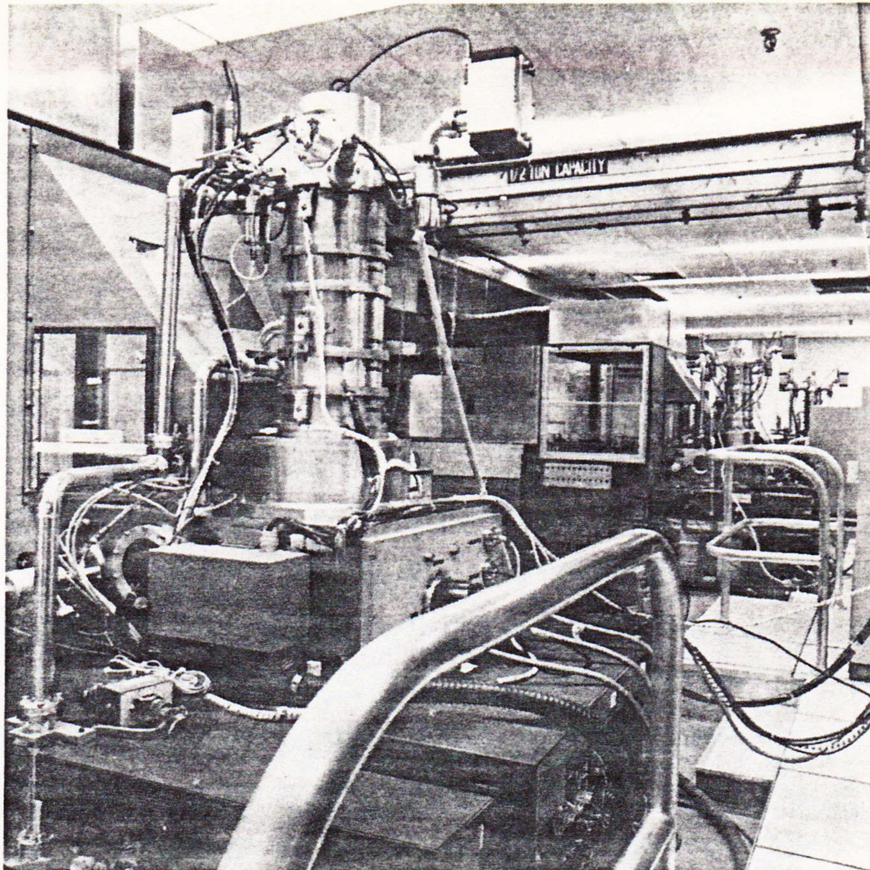


1. Electron-beam line. Electron-beam lithography systems of the EL-1 type on this semiconductor production line at IBM's East Fishkill, N. Y. facility have a throughput of 22 silicon wafer exposures per hour for 57-millimeter wafers with 2.5-micrometer lines and spaces.

Scanning electron-beam system turns out IC wafers fast

by E. V. Weber and H. S. Yourke, *IBM Corp., Hopewell Junction, N. Y.*

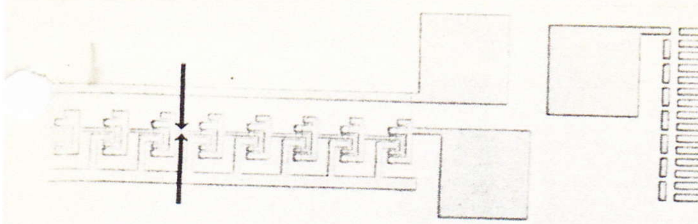
☐ Sometimes the answer to achieving the ever smaller geometries needed in semiconductor pattern-making is 'think big.' So it is with the first scanning-electron-beam system that achieves the throughput necessary for commercial chip production. The EL-1 (Fig. 1) scans the wafer with a square beam that covers much more of the surface than the round beam of other scanning systems. Thus more of a pattern can be exposed in an equivalent time, and wafer throughput rises dramatically. This one-of-a-kind machine points the way to commercial wafer production by electron-beam lithography.

The principal advantage of electron-beam lithography over optical lithography systems is that it avoids the limitations of resolution and depth of focus imposed by the wavelength of light. Scanning systems, which rely on computer control rather than masks to form the pattern, also have a high degree of pattern flexibility. For example, etching different patterns on adjacent areas of a wafer is accomplished easily and quickly. Moreover, eliminating the mask used in contact and projection optical lithography systems saves time and reduces errors and defects.

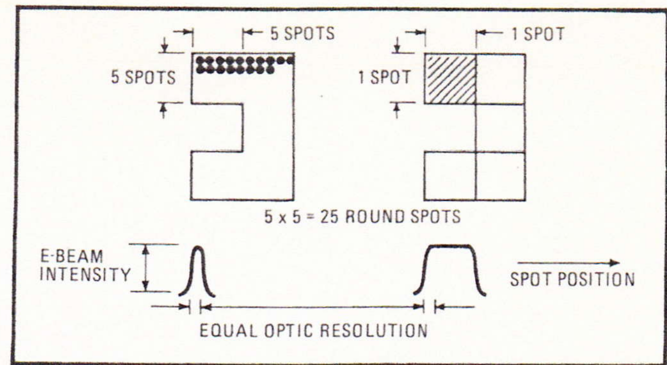
Scanning systems also make it possible to control microscopic pattern distortions in real time. Finally, they excel in overlaying new patterns on previously etched levels of a chip. An example of a high-quality pattern of 2.5-micrometer dimensions that was produced by a scanning system is shown in Fig. 2. [For a full introduction to electron-beam technology, refer to *Electronics*, May 12, p. 89.]

Raising throughput

The principal obstacle to full deployment of scanning systems in integrated-circuit production has been the difficulty of achieving the necessary throughput for cost-effective use. The throughput for the two commercially available scanning machines is only about one exposure an hour. Of course, these machines are primarily intended for mask making, but their production rate gives an idea of the distance that is to be traveled to meet



2. **Small patterns.** High-quality integrated-circuit chip was exposed by the electron-beam scan of the EL-1. Minimum conductor widths, such as in the line segment shown between arrows, are 2.5 μm. With minor modifications, this machine will be able to expose 1-μm lines.



3. **On the spot.** Other electron-beam lithography systems scan the image of IC patterns with a small circular spot. In the EL-1, a square spot equivalent to many circular spots is scanned across the silicon surface of a wafer. This procedure drastically cuts exposure time.

IC makers' standards of 20 to 30 exposures an hour.

The alternative electron-beam solution to the throughput problem is a projection system. Masks are used in such systems to expose all image points on a wafer at one time. While projection-system development is still under way, the problems of mask fabrication and handling have slowed progress toward a practical machine.

The EL-1 may be seen as a compromise: it uses the principle of the bigger exposure area found in projection machines together with the maskless flexibility of scanning units. In most other scanning systems, the beam is pencil-shaped, which gives a limited, round coverage of the wafer area. The square beam of the EL-1 produces an image as big as the smallest pattern element to be constructed—much bigger than other scanning systems' beams. The result is a throughput of 22 wafer exposures an hour, based on 57-millimeter (2¼-inch) wafers with 2.5-micrometer geometry.

Putting it to work

First use of the EL-1, at IBM's East Fishkill facility in Hopewell Junction, N. Y., has been for the production of bipolar large-scale integrated circuits. The unit's ease of data transfer, quick turnaround, and ability to balance inventory by mixing different patterns on a wafer make electron-beam exposure economically attractive even for IC patterns with line widths thick enough to be exposed with light optics.

Rapid pattern exposure is achieved by scanning a small, square wafer area, called a field, with a square projected image, called the spot. The sides of the spot are as long as the smallest dimension of the pattern that is being exposed. At a given current density, a 2.5-μm square spot is equivalent to a 5-by-5 array of 0.5-μm round spots, but it requires only 1/25th the exposure time (Fig. 3).

The square spot scans the field in a stepped fashion, moving from one grid on the field to the next by magnetic and electric deflection. When the scan of the field is complete, the stepping table that holds the wafer moves it so that the adjacent unexposed field is within the deflection range of the beam.

The field-scan procedure (top of Fig. 4) produces an exposure with an edge gradient equal to the beam's edge slope (defined as the distance from the edge of the spot that the beam's intensity takes to rise from 10% to 90% of its full value). In practical implementations, the square-beam approach provides better than an order-of-magnitude advantage in writing speed over other scanning systems.

Because limiting a pattern to a design made on a grid equal to the minimum line width of that pattern would be unduly restrictive, an offset capability is included in the EL-1. Spots may be displaced from their nominal location in increments of ⅕ of a spot (bottom of Fig. 4).

The electron-optical column that focuses and shapes the beam is designed to provide the maximum beam current and field size at the required edge slope. For instance, placing the deflection coil within the projection lens minimizes chromatic and electron-electron-interaction effects that result from the large currents used. Dynamic correction of focus and astigmatism keeps edge slope to less than 1/10,000 the length of the field.

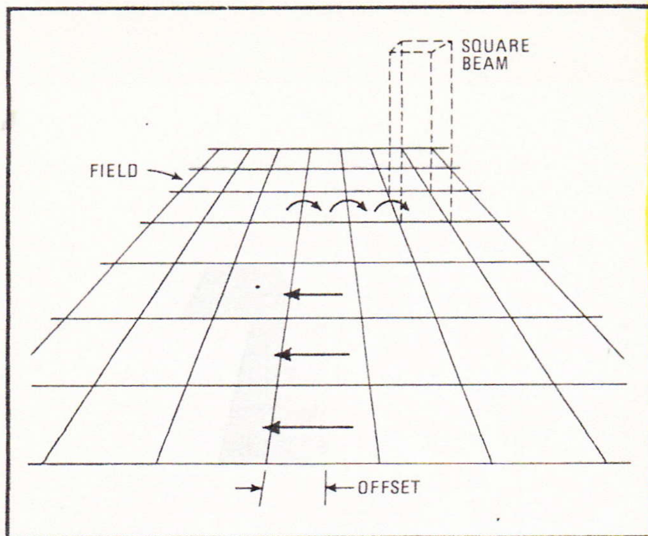
To obtain a workable lithographic tool, many engineering tradeoffs were necessary among such key performance parameters as throughput, edge slope, field size, current density, and overlay. Moreover, the applications in which these machines are used may influence these parameters. For example, field size when exposing chips smaller than 5 mm on a side is best adjusted to equal the chip size. On the other hand, larger chips are easily fabricated by the use of interstitial registration marks that make it possible to stitch adjacent fields together with optimum overlay and throughput.

A set of performance specifications for the EL-1's initial application at East Fishkill is listed in the table. As product requirements demand, the system may be adjusted to make exposures with dimensions that are in the 1-μm range.

On the spot

The square spot as big as the smallest pattern dimension is the chief design feature giving the system its rapid exposure rate. But to achieve this high throughput and to get good overlay (layer-to-layer registration) and large exposure field sizes, other features play an important role. Among them:

- Advanced electron optics to obtain high beam current for quick large-field exposures with high resolution.
- A combination of narrow- and wide-bandwidth deflec-



4. Checkerboard scan. For exposure purposes, a field is divided into a matrix of small squares. The shaped electron beam is stepped to each square in the matrix. It can be offset to expose lines centered on a grid of finer resolution than spot size.

tion of the beam for a good signal-to-noise ratio.

- A deflection cycle that repeats itself exactly, thereby ensuring that any errors are reproduced exactly—which aids error correction.
- Automatic measurement of deflection errors and compensation for them in order to attain maximum pattern accuracy.
- Four-mark registration with an associated deflection modification to give optimum overlay of patterns and to permit matching of boundaries on adjacent fields.
- A three-step highly automated sequence for wafer handling and alignment, which boosts throughput.
- Beam-deflection correction of errors in the position of the table that steps the wafer from field to field, thereby giving a high stepping speed and rapid settling.
- Use of servomechanisms to maintain beam current, spot focus, and column alignment over long periods.

Combining deflections

Within a given exposure field, the electron beam is positioned chiefly by a large-range, narrow-bandwidth magnetic deflection. During writing, a bidirectional magnetic ramp (Fig. 5) deflects the beam in a bidirectional raster fashion. Superimposed on this ramp is a bucking sawtooth applied by a small-range, wide-bandwidth electrostatic deflection. This combination causes the beam to step. In addition, a small-range, moderate-bandwidth electrostatic deflection compensates for errors. Restricting these larger bandwidths to small ranges results in minimum deflection noise and minimum random pattern error.

The deflection cycle of the EL-1 is a three-part repetition. In standard operation, the cycle repeats even while a new wafer is being loaded. The object is a steady-state deflection, so that distortions due to eddy currents, thermal currents, etc., will repeat at all points.

During the registration part of the cycle (Fig. 6a), the computer scans the beam sequentially over the locations of four registration marks. During the writing part of the cycle (Fig. 6b), the beam scans sequentially over the entire field. Each possible location is addressed, with the computer blanking out the beam at points that do not require exposure. This approach ensures that pattern differences will not change the deflection history. In general, densities of LSI patterns are high enough so that, even though throughput is slightly less than for deflection that addresses only the points to be exposed, the decrease is negligible and is far outweighed by the increase in accuracy.

TABLE: EL-1 EXPOSURE SYSTEM SPECIFICATIONS

Field size (maximum writing)	5 mm
Spot shape	square
Spot size (50% intensity)	2.5 μm
Edge slope (10 – 90%)	0.5 μm
Beam voltage	25 kV
Beam current (at 50 A/cm^2)	3 μA
Overlay (3σ)*	0.5 μm
Throughput for 57-mm wafer (76 chips)	22 wafer exposures per hour
Writing grid	2.5 μm
Writing grid offset capability	0.5-μm increments

*the 3σ error between the centerlines of two patterns on different layers designed to be coincident.

The move part of the cycle is the time that it takes the stepping table to move the wafer to the next exposure field. During the move, a special deflection (Fig. 6c) is always executed. Occasionally, it is used in conjunction with a focus fixture in the electron-optical column for automatic sensing and correction of focus.

Righting deflection errors

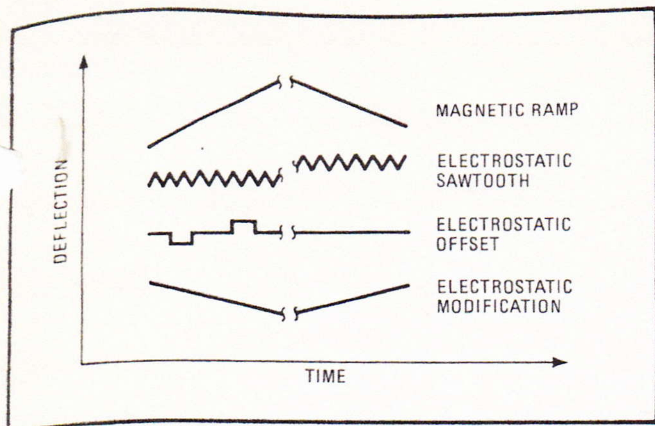
Repetitive deflection of the square beam gives the system its ability to define line widths and positions precisely. But repetition is not enough; the spots must be accurately positioned in order to obtain compatibility with different electron-beam or optical tools.

Accurate deflection is obtained by scanning a calibration grid on a special target and then compensating for sensed errors. The grid (Fig. 7) is an array formed by square openings in a layer of gold on a silicon substrate.

To measure deflection error, the grid is positioned on the stepping table, and the beam scans it. As the beam moves from the gold, which has a relatively high backscatter coefficient, to the silicon, which has a relatively low backscatter coefficient, the current changes in backscatter detectors. The time of this change is recorded.

A special program selects the times associated with selected grid points, edits and averages them to obtain centers, and then compares the results with a table of expected centers to obtain the deflection error. The table is based on calibrated locations of the grid marks on the target being used; thus the grid does not have to be perfect.

The error figure goes into programs that generate piecewise-linear corrections to the deflection. Usually, the error-measurement program applies previous corrections when directing the beam over the grid, and the new corrections are applied to the earlier ones. This iterative



5. Combined scan. A combination of narrow-bandwidth magnetic deflection and wide-bandwidth electrostatic deflection precisely positions the electron beam. This combination scan reduces deflection error and noise to acceptable manufacturing levels.

procedure minimizes the accuracy required of the correction electronics, since it does not permit errors to accumulate. Typical errors before and after correction are illustrated in Fig. 8.

It also is necessary to coordinate the registration scan, when the beam checks four registration marks on the wafer, with the subsequent write scan. The calibration target comes into play here, too. After the correction process just described, which is a writing-scan correction, the program calculates the expected positions of several grid points designated as test registration marks—basing these calculations on a write scan of the grid. Then the electron beam operates in the registration scan mode to locate these registration marks, and the difference between the observed and the calculated positions is sensed. This error information is stored and used during registration to adjust the sensed positions of the wafer registration marks so that they correspond with the writing scan.

These measurements and corrections of deflection errors bring the field being scanned on the wafer to within 30 parts per million of ideal. However, ideal deflection may not achieve optimum overlay of successive patterns required for the manufacture of semiconductor devices. Some causes of deviations from the ideal are: imperfect mechanical positioning of the wafer on the table, wafer distortions caused by processing, and inaccuracies in previous patterns.

As in any photolithographic process, accurate registration is essential for optimum overlay of successive patterns on a chip and to properly mesh adjacent exposure fields on a chip. With the EL-1, registration goes a step beyond simple mechanical adjustment to registration marks, and the scanning beam is adjusted to them.

The system achieves optimum overlay by locating the registration marks in the four corners of the previous pattern and adjusting magnification, rotation, translation, and shape of the field to match it to the marks. Typically, the marks are features formed as a byproduct of earlier processing.

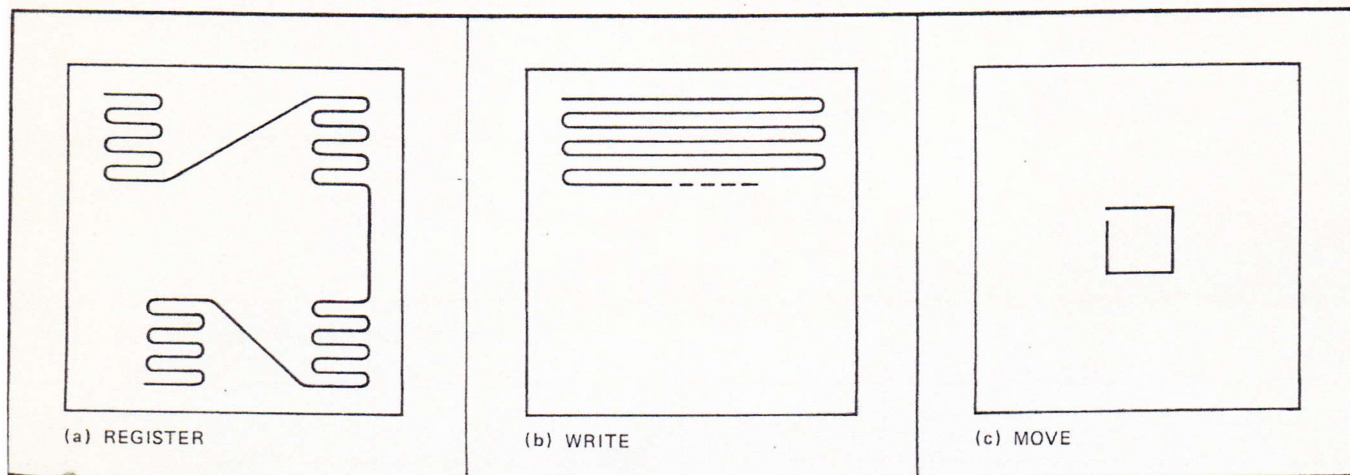
Registration gives accuracy

The detection process is quite similar to the one used in deflection correction. It depends upon the fact that the energy distribution and quantity of back-scattered electrons are essentially constant when the beam scans a flat surface, but change when the beam crosses an edge formed by a change in material or by the topography of the wafer surface. Automatic gain-control circuitry compensates for wide signal variations between wafers of different types and between different processing levels on a given chip.

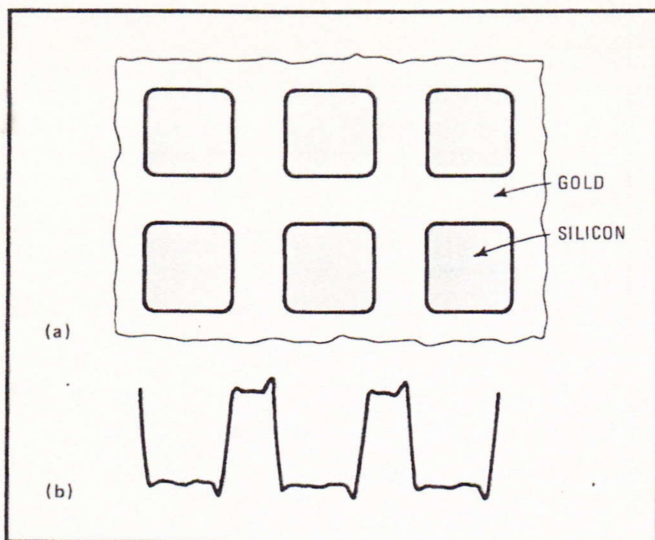
Each time the signal crosses a registration edge, special circuitry transmits the time to the control computer. To identify each of the marks, the computer edits the sequence of time samples and correlates it to a model. Then deflection modifications are generated to match the writing field to the registration marks.

The average error of magnification is used to obtain an approximation of height errors and to form a focus correction. Even though depth of focus is an order of magnitude greater than for light optics, this correction helps achieve accuracy.

The maximum size of the exposure field is limited, but chips can be made of more than one field—as large as a whole wafer, even—by stitching fields together. Marks



6. T[illegible] step. A repeating three-part deflection cycle maintains distortion constant over all points in a field. First step (a) is a registration scan followed by a writing scan (b) over the entire field. Last is a move cycle (c) in which the beam steps to a new field.



7. Calibration. A grid consisting of an array of square openings in a layer of gold on a silicon substrate (a) is the reference for the EL-1's circuitry for deflection error compensation. Signals (b) from the gold's high backscatter yield errors in grid position.

between adjacent fields are shared, thereby making their boundaries coalesce.

The system can write a new registration mark before an earlier one degrades to the point of unusability. Space is allocated for rewriting a mark three times, each at a new location. In some cases, rewriting can take place at a previously used location.

This four-mark registration is the final step in a three-part sequence designed to provide progressively finer adjustments of the wafer's alignment to the beam. First, as wafers enter the EL-1, a mechanical handler places them on carriers and subsequently positions them under the beam. The positioning locates the wafer relative to the beam to $\pm 75\ \mu$m.

The second step is a registration process involving the entire wafer. It adjusts the magnification and rotation in the individual field to provide an alignment of wafer and beam within 2μm to $5\ \mu$m of each other. The necessary registration data is obtained by scanning two special marks on the wafer. Third, the four-mark registration procedure further positions and modifies the writing field to obtain an overlay of better than $\pm 0.5\ \mu$m.

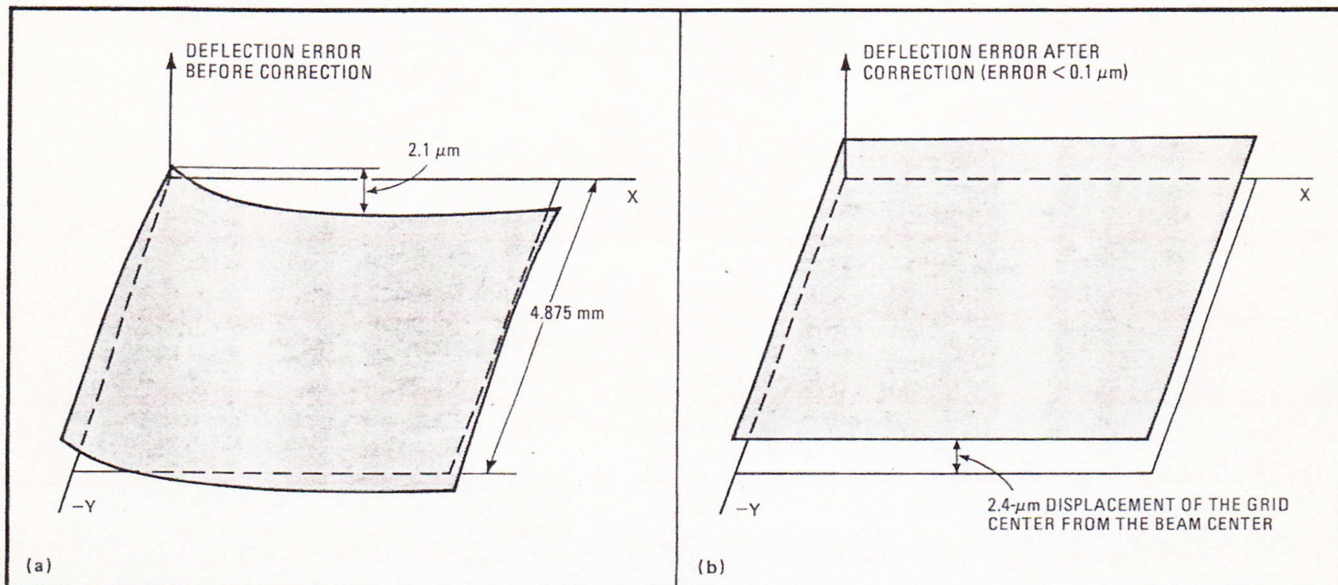
To provide rapid stepping of the table as it moves the wafer from one field to the next, a dc servo motor drive smoothly accelerates and decelerates to a stop without hunting for a precise position. Design emphasis was on rapid settling of the table to within $\pm 7.5\ \mu$m of the desired position. Then a beam deflection in response to a position encorder achieves beam-to-table accuracy better than $2.5\ \mu$m. This two-prong approach makes it possible for the table to move 5 mm to another field and settle within 250 milliseconds.

Load and unload

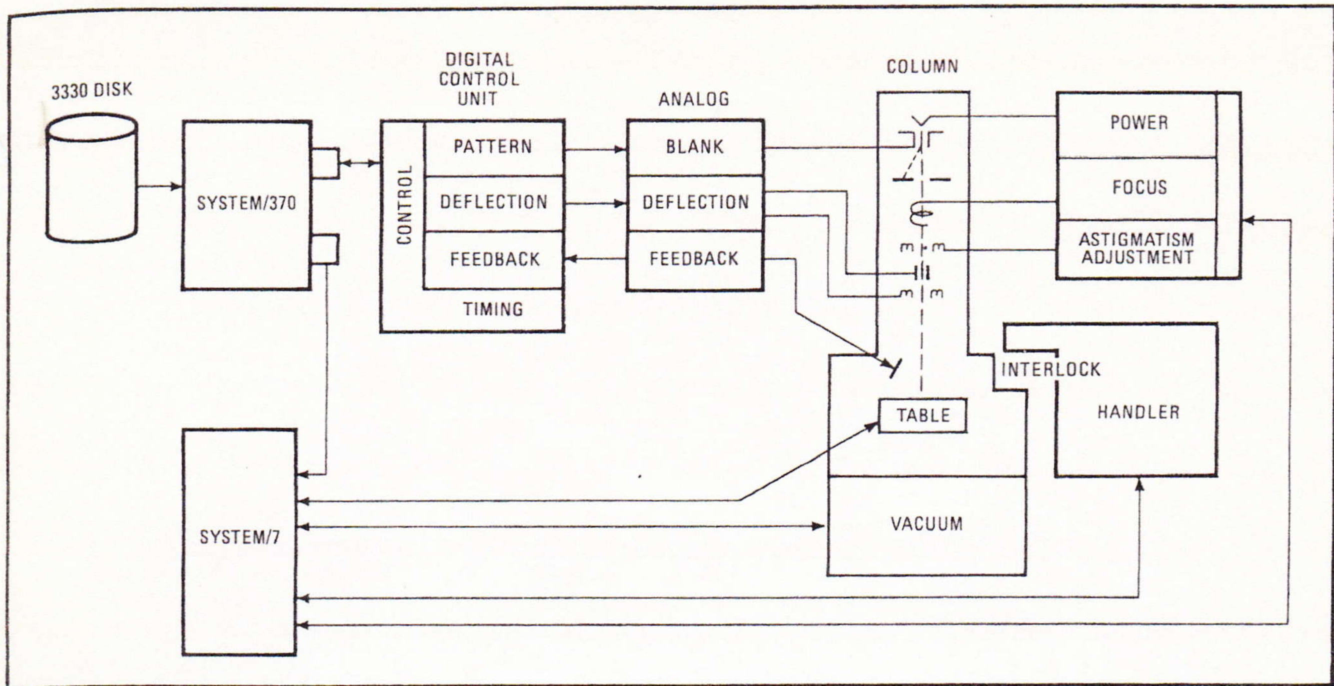
Another design feature that speeds the production rate is a vacuum interlock combining the wafer transport with the valving mechanism that removes the air. The volume of air that must be removed is small enough so that the system can be rapidly pumped to an intermediate volume, then opened to the large main chamber, which is at vacuum, giving a transition from atmosphere to 10^{-6} torr in 4 s. This combination of transfer and interlock makes it possible to exchange a wafer on the stepping table with the next wafer that is at atmosphere in about 15 s.

Another feature that insures maintenance of high throughput is a set of servomechanisms that monitor and adjust alignment of the electron-optical column and parameters of the electron-beam gun during the period in which the table is stepping the wafer from one field to the next. These servomechanisms insure satisfactory exposure quality over long periods of time. Periodically, the edge definition of the beam is monitored by the scanning of a focus target.

The various components of EL-1 go together as indi-



8. Deflection correction. Typical three-dimensional plots of X deflection error before and after correction (a and b, respectively) show how a scanning system can electronically correct itself. In this case, a 2.1-μm error is reduced to less than 0.1 μm.



9. Automated electron-beam. The major components of the EL-1 are a vacuum beam-producing column with an automatic wafer handler, a digital control unit, analog correction circuitry, and an IBM System/370 plus magnetic-disk memory as the central controller.

cated in Fig. 9. A System/370 computer is the central control element. The principal information store is a 3330 disk storage, containing such key data as pattern descriptions, wafer maps describing pattern types and locations on the wafer, descriptions of deflection patterns to define field size, and the locations of registration marks.

As part of system preparation, a deflection path suitable for writing a pattern, is transferred from disk to the deflection memory in the digital control unit. Under control of the system clock in this unit's timing section, the deflection data causes a sequence of digital control signals to be transmitted to the deflection circuitry in the analog unit.

Beam drive

This circuitry in turn produces the appropriate drive for the beam to follow the paths of Fig. 6. Once the deflection has stabilized, the System/370 control program causes the table to move the calibration target under the beam, transmits a pattern to the pattern section of the digital control unit, and activates the feedback sensors. When the beam is in the vicinity of the selected grid marks, the pattern section unblanks it. Back-scatter signals are processed by hardware and software to form the set of deflection corrections, which are placed in the correction memory of the digital control unit.

When the deflection has been corrected, the system is ready to write on the wafers. The operator tells the control program for the System/370 which wafer map to use. The control program initiates the transfer of the first wafer to the stepping table via a System/7 computer, which interfaces and monitors the subsystems. The wafer registration mark specified in the wafer map is then moved under the beam.

After the three-step registration cycle is completed at the first field, the pattern defined by the wafer map is called out, the field is corrected on the basis of the registration information, and the pattern is written.

The wafer moves to the next field site, and the sequence of four-mark registration, write, and move repeats for each of the fields on the rest of the wafer. Patterns could differ at each exposure, depending on what is specified in the wafer map. When the last exposure is completed, the table may move to the focus target or the calibration target to collect data and determine whether focus or deflection has drifted enough to call for an update. Such updates to corrections are required only infrequently.

If the following batch of wafers requires a different field size, an appropriate deflection and the corrections previously acquired for that deflection are loaded. The corrections are checked, but the previous corrections usually are adequate, so writing proceeds without correction convergence. Numerous different deflection cycles are available to optimize field size and accommodate different registration marks.

Small dimensions

For the past three years, the EL-1 has been successfully exposing bipolar patterns on silicon wafers. High-quality images with minimum dimensions of 2.5 μm and layer-to-layer registration of well under 0.5 μm are being routinely achieved in the large-scale production of bipolar wafers.

In the future, this capability could easily be extended to pattern geometry with 1-μm detail. Addition of higher-speed data-conversion circuitry to raise throughput to even higher levels and a redesigned wafer staging area for handling larger wafers are other possible system improvements. □