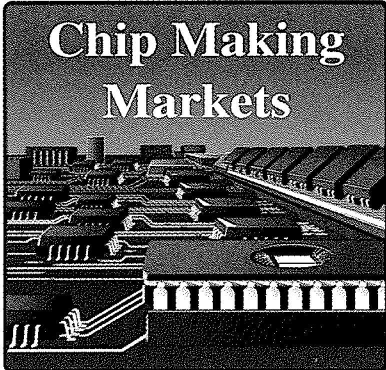

Impact Appraisal

Please file in Volume I1 behind the appropriate tab.

BEOL Wiring Process For CMOS Logic

February, 1995

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Notes

Overview

- **Low permittivity dielectrics will be used for 0.25 micron processes.**
- **Sputtering is holding on at the expense of CVD.**
- **CMP is becoming the favored choice for planarization.**
- **Copper is the favored emerging interconnect material.**
  - **But it will stay in R&D through the 0.25 micron generation.**

The term BEOL is relatively new to the industry. Nevertheless, the markets created by BEOL processes are already the most sought-after in the equipment industry. The BEOL, or Back-End-Of-the-Line, comprises all the process steps used for forming the metal interconnects including the dielectric before the first global interconnection film is deposited. The primary purpose of BEOL processes are to wire together all the transistors put down in FEOL (Front-End-Of-the-Line) processes. **BEOL processes are the physical embodiment of a chip maker's intellectual property**. Properly implemented, they allow a chip maker **to integrate more at a low cost.** This in-turn, gives a chip maker **greater product differentiation, which adds value. These factors make BEOL processes critical to a chip maker's profitability**.

The major players in the world's chip industry are gearing up for the incoming 0.25 µm era. This new era will create tremendous opportunities for chip makers and equipment companies alike. At the center of this opportunity will be the competition for BEOL film technology. This Impact Assessment describes BEOL, the thin films which it encompasses, and the trends that are likely to develop. VLSI Research has compiled the results from the roadmaps of the 13 largest chip makers in the United States, Japan, and Korea in an effort to shed some light on recent technical trends. The technical issues pertaining to multilayer wiring in high speed CMOS circuits are discussed below.

BEOL and FEOL Processes

- **A consistent set of definitions for BEOL & FEOL thin films is developed.**
- **BEOL processes are used to form global interconnect.**
- **FEOL processes are used to form circuit elements and local interconnect.**

One of the first issues encountered when attempting to unravel the complexity of current day processes is the technobabel used. It can gray the hair of even the most seasoned technologist. **There are many acronyms and terms that have evolved with no agreed-upon, industry-wide, definitions.** One company's BEOL film can be another's FEOL film. A good example of this is the acronym PMD. For some it means Poly-Metal-Dielectric, for the dielectric film used to insulate the last polysilicon film from the first metal film. For others, it means Pre-Metal-Dielectric, which can mean the same as the former, or it can include all the CVD dielectrics deposited between the gate conductor and the first metal conductor. For still others, it can mean Post-Metal-Dielectric, for all the CVD dielectrics deposited after the first metal conductor. There are similar problems with terms such as BEOL, FEOL, ILD and IMD. It is easy to see why things get so confusing.

So **it is essential to first establish fixed definitions** for the films and their requirements used in BEOL and FEOL processes, before attempting to discuss them. The definitions chosen here will represent what we at VLSI Research believe represent the majority view within the industry, even though they may not be completely consistent with any, one, company's definitions. In those instances, where there are no commonly accepted terms, we have chosen terms that make the most sense. The purpose of this section then is to develop a common set of definitions that can be used when discussing thin films used in semiconductors. **A glossary is included in the back of this document for further clarification.**

FEOL stands for Front-End-Of-the-Line. **BEOL** stands for Back-End-Of-the-Line. **Neither should be confused with the term 'front-end' or 'back-end.'** 'Front-end' refers to all of wafer processing, while 'back-end' refers to test and assembly. FEOL and BEOL are subsets of just the front-end, or wafer processing.

The terms FEOL and BEOL originated at SEMATECH several years ago as an attempt to describe the growing differences between processes for logic circuits and those for DRAM circuits. SEMATECH's constituency was largely made up of companies focusing on logic circuits, while competition in Japan was largely focused upon DRAMs. But, DRAMs were becoming ever more specialized and not as indicative of processes encountered among SEMATECH's constituents.

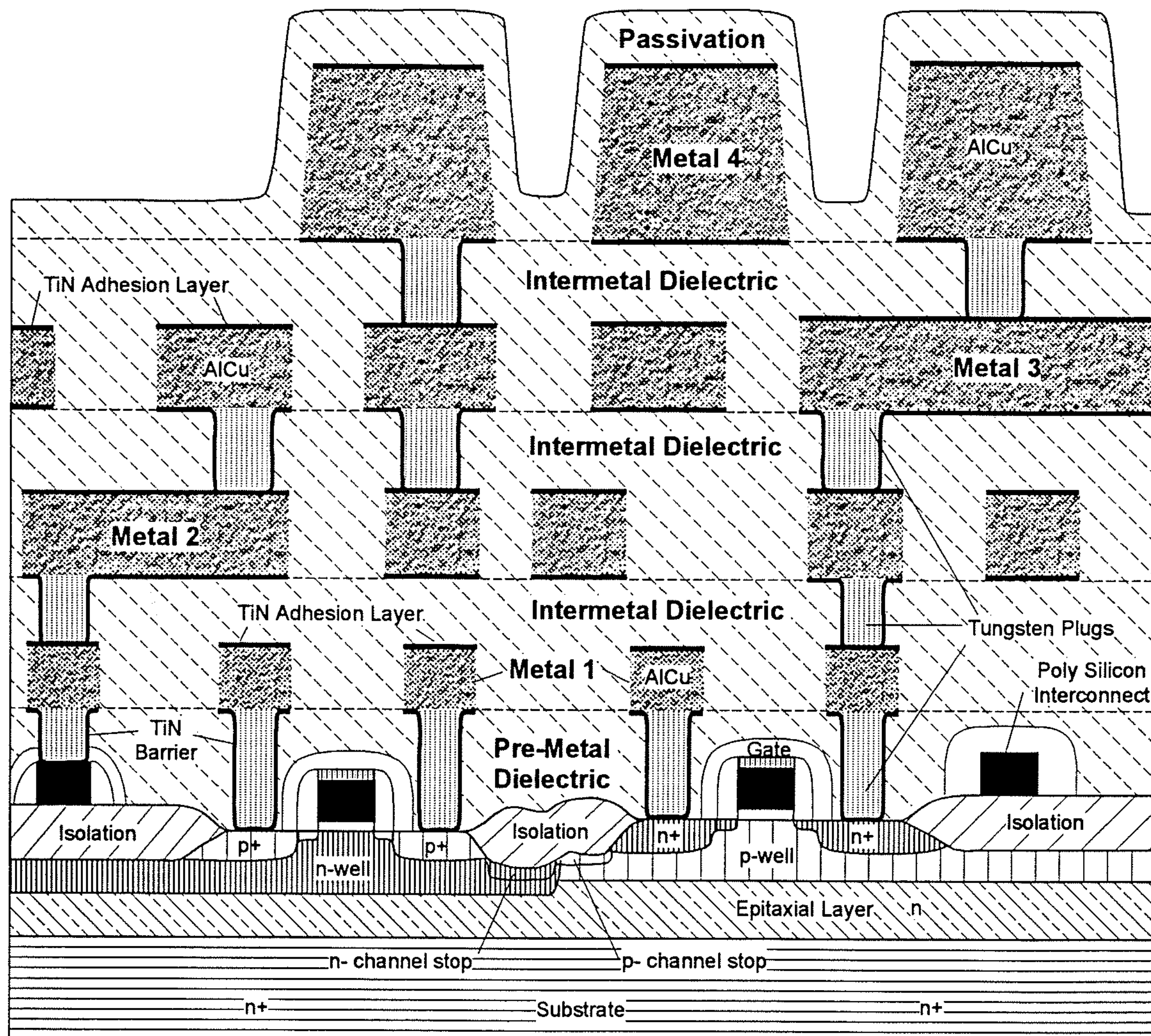
When one speaks of BEOL intensive circuits, he or she is usually referring to those processes developed for logic circuits. However, **BEOL intensiveness is not limited to just logic**. Advanced SRAMs often have three or four metal interconnect layers as well.[1] **BEOL intensive circuits** such as microprocessors, ASSPs, and ASICs **have complex metal interconnect structures**, but simple transistor and capacitor structures. This can be seen in presentation 1, where the quantity of metal interconnect layers dwarf that of the transistors. The insignificance of FEOL processes to manufacturers of BEOL-intensive circuits can be seen in drawings of their circuit

[1] SRAM processes are very similar to logic processes. Many chip makers find them ideal process drivers to improve yields in their logic processes.

Presentation 1

A BEOL Intensive Circuit

(Back End of the Line)



Source: VLSI RESEARCH INC
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cross sections. These seldom contain capacitors, resistors or local interconnect structures, only transistors. These circuit elements are also used in BEOL intensive circuits, it's just that their manufacturing is not technically challenging and need not be shown.

In contrast, when an individual speaks of FEOL intensive circuits, he or she is usually referring to those processes developed for DRAMs. But as previously mentioned, **FEOL intensity is not limited to just DRAMs**. Rather, EPROMs, flash memories, and mixed signal circuits also often have complex FEOL processing steps, with relatively few metal interconnect layers. **FEOL intensive circuits have complex transistor and capacitor structures**, but simple metal interconnect structures. This can be seen in presentation 2. Here transistor and capacitor structures made in the FEOL, impose upon the BEOL interconnect structures which are shown in bold. Makers of FEOL intensive circuits tend to downplay the significance of BEOL processes in their drawings of circuit cross sections. They seldom depict more than one BEOL interconnect layer. Unlike BEOL intensive chip makers, however, FEOL intensive chip makers do find BEOL steps to be technically challenging. But the challenges are different. **FEOL intensive chip makers are much more concerned with the cost of the BEOL process. In contrast, BEOL intensive chip makers view BEOL complexity as a way to add value to the chip. These differing objectives lead to significantly different approaches in the respective BEOL processes.**

The differences between FEOL and BEOL intensive circuits are significant. Moreover, they cannot easily be lumped together into existing market segments because they cross the boundaries between memory and logic. This had prompted the industry to adopt FEOL and BEOL terminology as an important way to differentiate semiconductor technology. The dividing line between both is depicted in presentation 3. **FEOL** comprises all those wafer process steps commencing from when the wafer starts into production and lasting through that conducting layer put down just before deposition of the first metal layer to be used for global interconnect. It **includes all the films needed to form transistors, capacitors, resistors and local interconnects.**

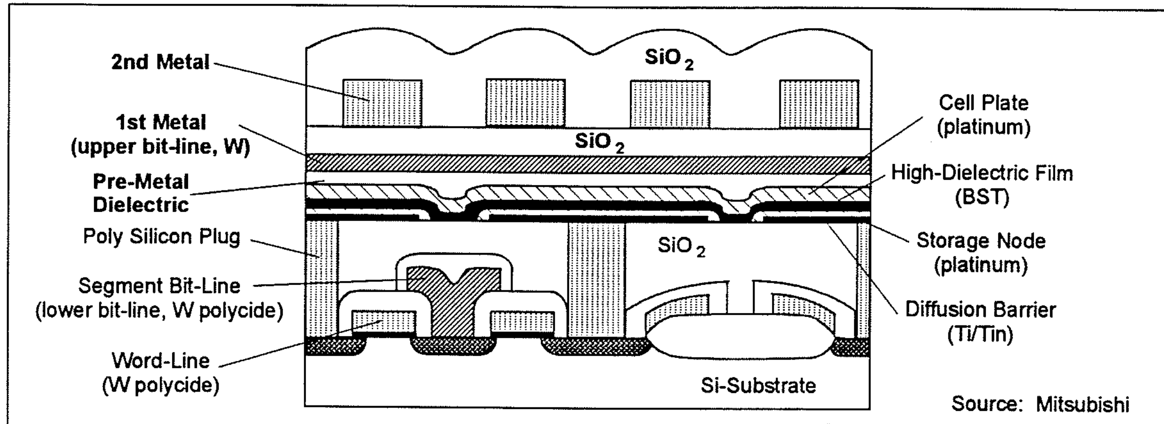
Local interconnect includes conductors used to form straps, short word lines and short bit lines. These are usually composed of doped polysilicon, in order to withstand the high temperatures used in FEOL processes. However, polysilicon resistivity is usually too high to conduct signals well over long paths. **Local interconnect will** therefore **connect those circuit elements that are very close to each other, or it will be used to strap to global interconnect wiring.**

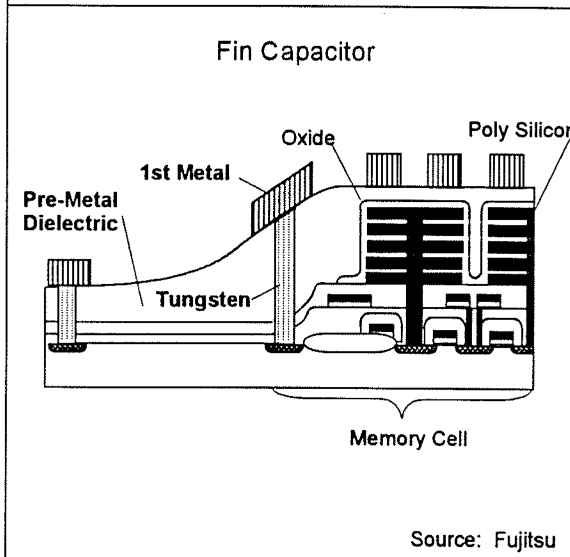
Global interconnect wiring is usually deposited with aluminum alloys or other metals which have high conductivity, so that signals can traverse the long paths across the chip. **The BEOL comprises all those process steps used for forming global interconnections, including the last dielectric just before the first metal film to be used for interconnection. VLSI Research has chosen to call this the Pre-Metal Dielectric or PMD film.** There are no other films in a device that will make use of that term. Metals are always used for global interconnection because of their high conductivity. **The primary purpose of BEOL processes are to connect together transistors and those other elements put down in FEOL processes.**

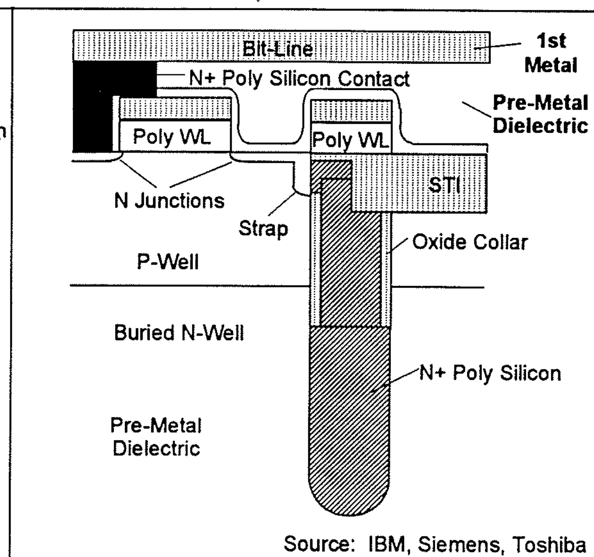
Presentation 2

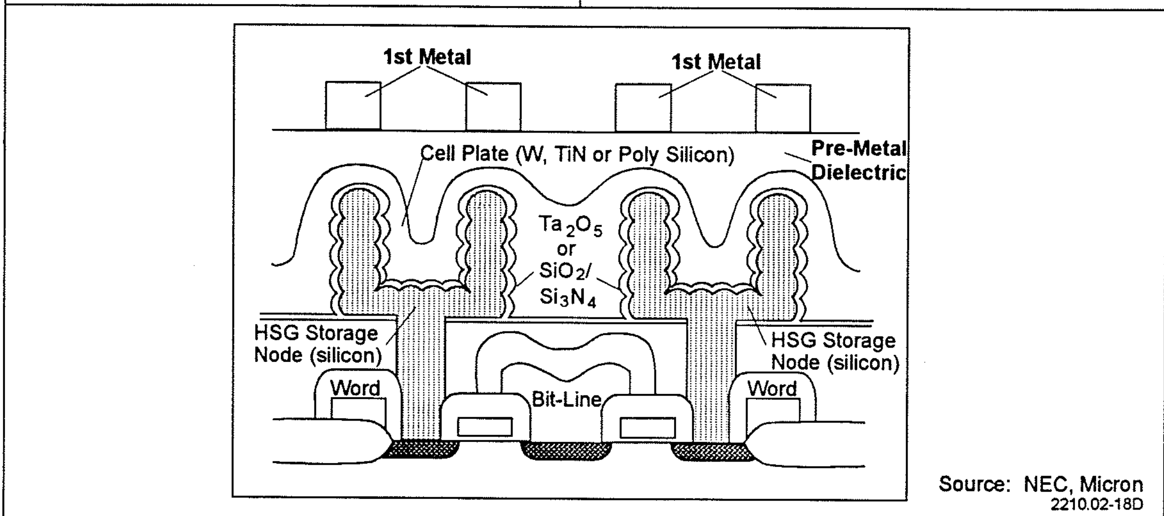
256 Mbit DRAM Cell Structures

(BEOL steps in **Bold**)



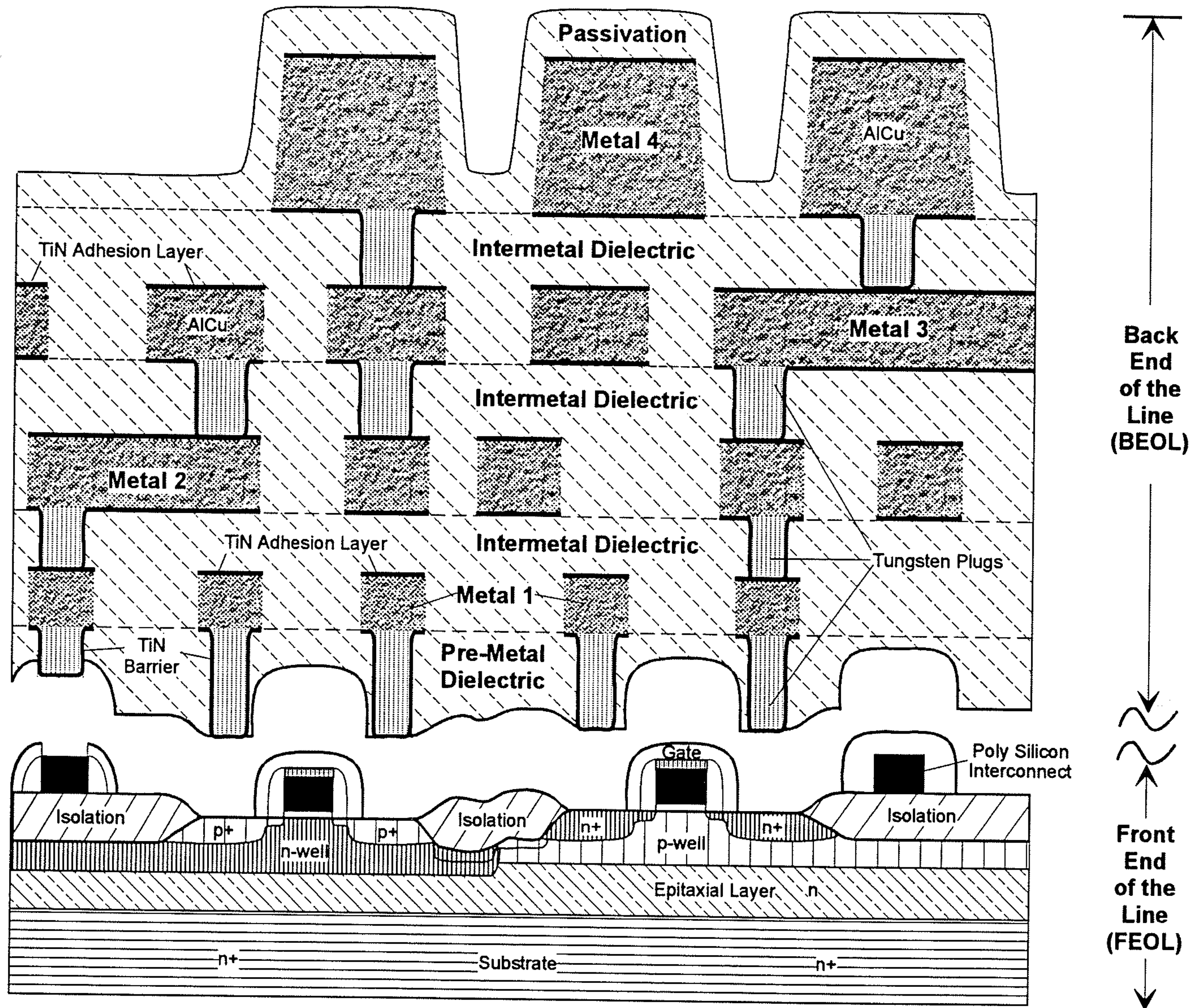






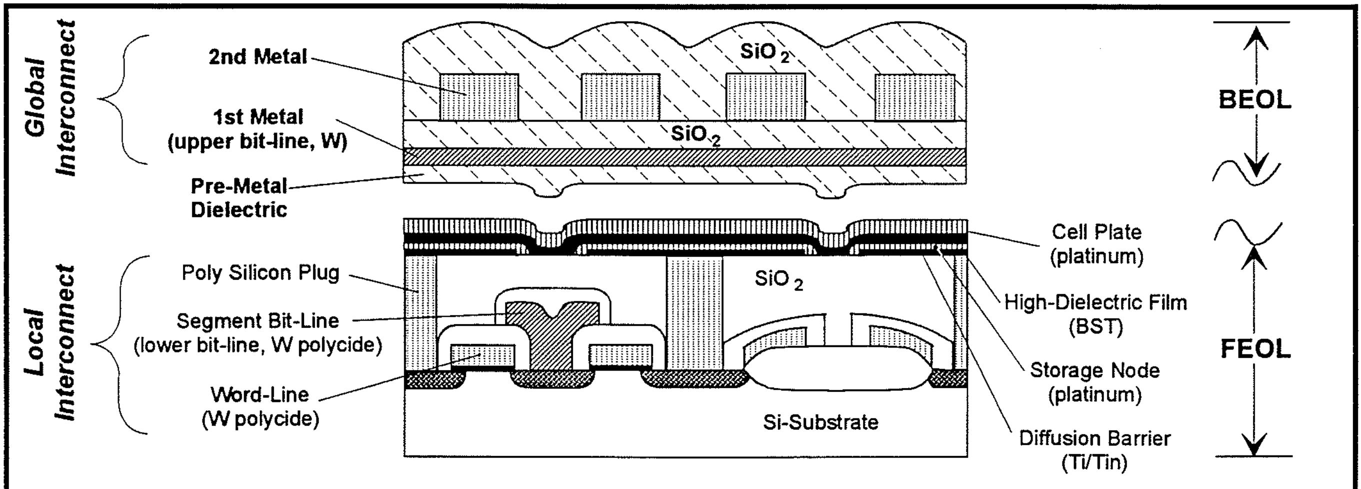
Presentation 3

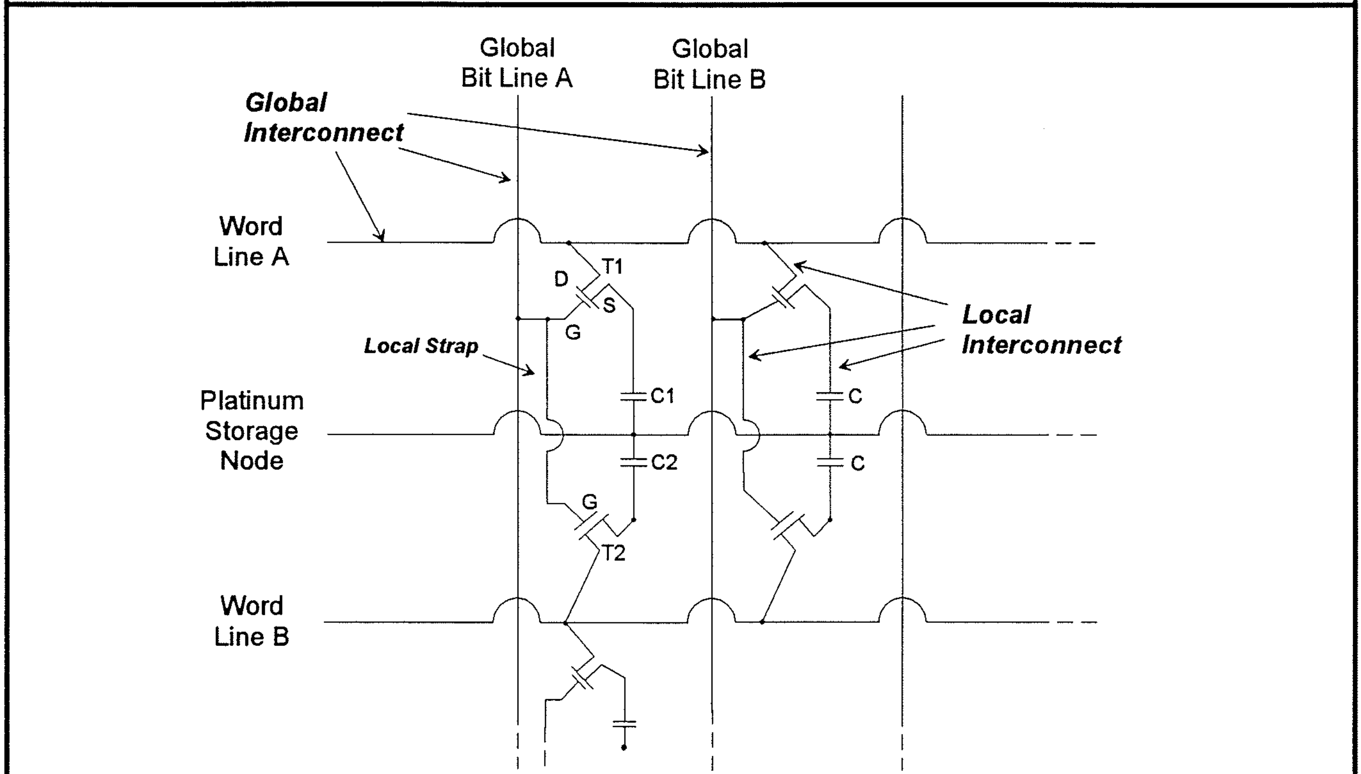
Cleaving BEOL from FEOL

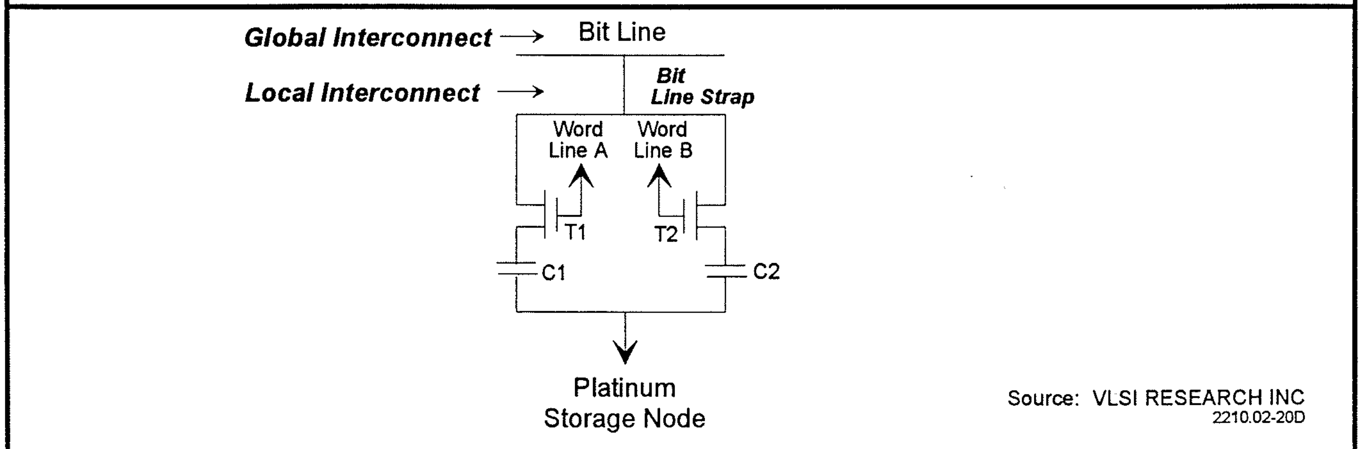


How these relate physically and electrically in a modern DRAM circuit from Mitsubishi is shown in presentation 4. The top third of the drawing shows how BEOL can be easily cleaved from the FEOL. The global interconnect wiring is made with the first and second metal films. The local interconnect wiring is made with polysilicon films and tungsten polycide films. The center of presentation 4 depicts two CMOS cells laid out horizontally under the global interconnect. The bottom of presentation 4 shows an electrical diagram of a single CMOS cell. In each case, the cells and local interconnect are separable from the global interconnect and other BEOL films.

Mitsubishi's 256 Mbit DRAM Cell Structure and Layout







Source: VLSI RESEARCH INC
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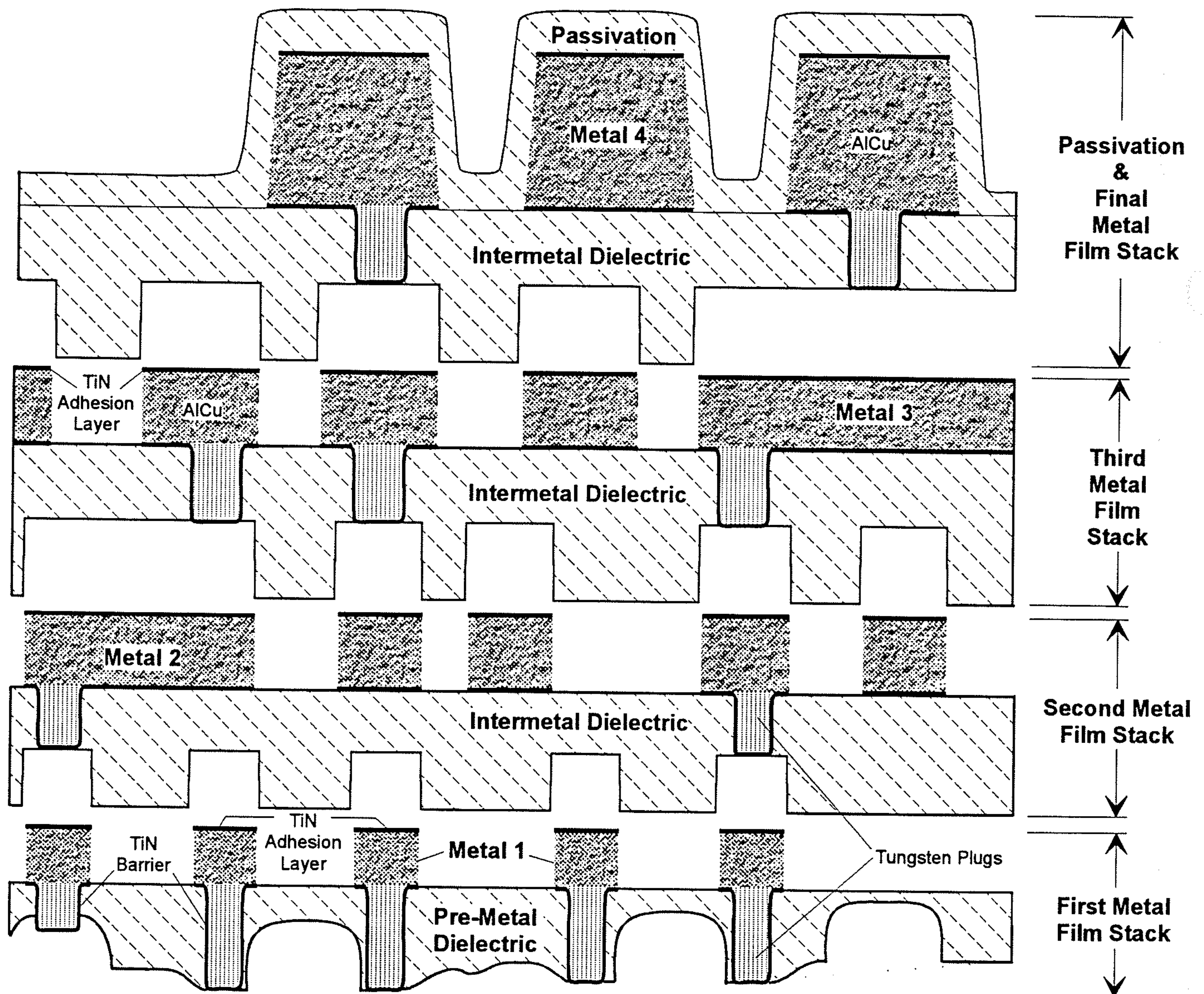
Advanced BEOL processes will typically include four or five global interconnect films, an equal number of conductor films (metal), interlayer dielectrics, barrier layers, adhesion layers, plug layers and a passivation layer. The films comprising each level of global interconnection are often combined into a single set and called a film stack (see presentation 5). **Film stacks are usually comprised of an interlayer dielectric (usually SiO_2), a barrier film[2] (usually TiN), a plug layer (usually W or AlCuSi), a conducting film (usually AlCuSi) and an upper adhesion film (usually TiN).**

Plugs can be filled in a separate step with a film that is different from the interconnect layer, or they can be filled with a film that

[2] Which also serves as a lower adhesion film.

Presentation 5

BEOL Metal Film Stacks



is the same as the interconnect layer in the same step. The most common example of the former is a W-plug AlCuSi sandwich film. The most common example of the latter is a AlCuSi-reflow film in which the aluminum is flowed into the via to form the plug.

The first metal film stack is substantially different from the others in that it has the tightest linewidths, the deepest aspect ratios, and the roughest topography. It is also different because the pre-metal dielectric (PMD) can be reflowed, which is not true of intermetal dielectrics.

The **passivation layer** is substantially different from intermetal dielectrics because it must protect the chip from the outside environment.

Trends in BEOL Film Usage

- **Most companies are focused on film stacks after the first metal.**
- **Low permittivity IMDs will be needed for 0.25 micron processes.**
- **CVD TiN is emerging.**
- **New sputtering systems promise to reduce process costs.**
- **Tungsten plugs and CMP are being designed out.**

BEOL films can be neatly segmented into processes for the first metal film stack, processes for all subsequent metal film stacks, and for the final passivation film. The first metal film stack differs from subsequent ones because of subtle complexities. Contact is made to the junctions; these contact windows can be very deep and narrow; surface topography is much more varied; planarization is critically needed; processing temperature is less constrained; film stress is less important. Still, geometries are set their tightest at this point. These subtleties are important because they determine the requirements for those films to be used in the first metal film stack.

Junction contact is important for two reasons: a barrier film must be present to keep aluminum from spiking into the junctions. It is also the lowermost point of contact that any metal film will have to make (refer back to presentation 1 for a graphic depiction of this). This latter point results in contact windows that are very deep and narrow in deep-submicron processes. Thus, **step coverage issues will be the most critical for the first metal film.**

Surface topography is much more varied before the first metal film stack is deposited because all of the circuit elements have been built up from the substrate by the FEOL processes. **Planar film surfaces are not as important in FEOL processes because CVD or diffusion is used for all of the film applications.** Both methodologies are conformal and introduce minimal step coverage problems. But the variation in surface topography accrues as these film layers are successively applied. This causes **the pre-metal dielectric to be the most important film to be planarized among all the films in a BEOL process.**

Pre-metal dielectrics are easier to planarize because processing temperature is not as constrained as it is with inter-metal dielectrics (IMD). Most FEOL processes can withstand the higher temperatures needed to reflow BPSG. This is not true

for those processes that use titanium salicide (self-aligned silicide) processes.[3]

Film stress is not as critical with pre-metal dielectrics as it is with inter-metal dielectrics. Stress in IMD films can lead to cracks, voids or hillocks in the underlying metal film. **Since stress is not as critical in the PMD film, thick ozone TEOS films can be deposited. These films offer excellent local planarization.**

The first metal film has the tightest geometries of all the metal layers. For example, Intel's 0.35 micron process uses the following critical dimensions for its metal layers:

Layer	Linewidth (microns)	Pitch (microns)
1st Metal	0.44	0.88
2nd Metal	0.58	1.16
3rd Metal	0.58	1.16
4th Metal	1.90	3.04

However, linewidths at the first metal layer present more of a dilemma for lithography and etch than they do for deposition. Lower film stress and thermal constraints make these films less challenging. The PMD dielectric can be reflowed, aiding step coverage for sputtering systems. As a result, **there are few new trends in film usage for the first metal film stack (see presentation 6). Most of the industry continues to favor ozone-TEOS films for the pre-metal dielectric. The trends in film deposition for the first metal interconnect and the contact plug favor reflow sputtering.**

Presentation 6

First Metal Film Stack

(anticipated usage in percent†)

Layer	Process	LINEWIDTH	
		0.35μm (%)	0.25μm (%)
Interconnect	TiN/AlCu/TiN	38	54
	TiN/AlCuSi/TiN	46	31
	AlCuTi	8	0
	Cu 0	8	
	W/TiN	8	8
	TiN/AlCuTi/TiN	0	0
Contact Plug	TiN		
	Sputter	92	46
	CVD	8	54
	Al		
	Conventional Sputter	8	0
	Reflow Sputter	31	31
	HP Sputter	8	15
	W		
	Selective	8	8
	Blanket	46	46
	Etchback	23	15
	CMP	31	46
Pre-Metal Dielectric	APCVD Ozone–TEOS	77	77
	PECVD	23	8
	LPCVD TEOS	0	8
	ECR PECVD	0	8
	CMP	46	69

†*Totals may add to greater than 100% because of multifilm sandwiches.*

Source: VLSI RESEARCH INC

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Film stacks after first metal are somewhat less critical because linewidths are usually larger and vias only connect to underlying metal or polysilicon layers. Additionally, while via windows are narrow, they are not as deep as are the contact windows on the

[3] The titanium salicide process is used to cap junctions and polysilicon. The titanium salicide process is being increasingly used by microprocessor vendors to make devices run faster. The titanium salicide process requires that titanium be deposited over the gate and junctions. This is then annealed to form a titanium silicide film. Process temperatures cannot exceed 800°C once a titanium silicide film has been formed. Otherwise, titanium silicide grains will grow, creating a roughness problem; the titanium silicide will also absorb dopants from the junctions, creating contact resistance difficulties, hence the desired ohmic contacts can actually become barrier contacts and will allow only one way current flow. Also, titanium silicide films are easily oxidized, creating a resistance problem. The advantage to using titanium silicide is that the sheet resistance of the junctions can be lowered from the normal 100 to 200 ohms-per-square to less than 2 ohms-per-square. This allows the device to run faster.

first metal. Surface topography is also not as critical if the first metal stack is planarized. This avoids expensive planarization techniques.

However, **film stacks after the first metal have different deposition constraints: processing temperatures and film stress must be kept low to avoid damaging underlying metal layers. Electrical performance issues also play significant roles in process choices. These constraints have created much more variety in the deposition methods being examined** (see presentation 7).

Dielectrics

The first BEOL dielectric is placed between the last FEOL conducting layer and the first metal layer to be used for global interconnect.[4] This is the pre-metal dielectric layer (PMD). **APCVD Ozone-TEOS continues to be the favorite dielectric for the first metal film stack** (refer back to presentation 6). The primary advantage is in its ability to planarize the Pre-Metal Dielectric layer (PMD). Ozone-TEOS films deposit with a high surface mobility, acting like a liquid—filling trenches and smoothing surfaces. APCVD provides better quality ozone-TEOS films than does PECVD, with less contamination. However, the high tensile stress of these films limit their application for inter-metal dielectrics.

With the exception of the final passivation layer, all the dielectrics used after the first metal film for global interconnect are intermetal dielectrics. PECVD SiO_2 films have been the IMD workhorse for nearly ten years.[5] PECVD will decline in use for

Presentation 7

Film Stacks after First Metal

(anticipated usage in percent†)

Layer	*Process*	*LINEWIDTH* 0.35µm (%)	0.25µm (%)
Interconnect	TiN/AlCu/TiN	46	54
	TiN/AlCuSi/TiN	46	23
	AlCuTi	8	0
	Cu	0	15
	W/TiN	0	0
	TiN/AlCuTi/TiN	0	8
Via Plug	TiN		
	Sputter	69	38
	CVD	0	31
	Al		
	Conventional Sputter	8	8
	Reflow Sputter	23	8
	HP Sputter	8	23
	W		
	Selective	8	8
	Blanket	54	54
	Etchback	23	15
	CMP	31	54
IMD Dielectric	TEOS based SiO_2	77	39
	PECVD	38	0
	PECVD, Low ε	8	31
	APCVD, Ozone-TEOS	31	8
	Other SiO_2	46	61
	PECVD	15	15
	High Density Plasma	31	46
	ECR	0	8
	Other HDP	31	38
	SiOF	0	16
	PECVD	0	8
	HD PECVD	0	8
	SiON, PECVD	0	8
	CMP	54	54
	Undecided	8	8

†Totals may add to greater than 100% because of multifilm sandwiches.

Source: VLSI RESEARCH INC

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[4] This dielectric film is often referred to as the PMD layer, or Pre-Metal-Dielectric.

[5] Applied Materials' P5000 success was largely based on serving this market.

deep-submicron processes due to its poor gap-filling abilities (see the lower third of presentation 7). Use of APCVD to deposit IMD films will also decline. **The relative high permittivity of SiO_2 films also creates difficulties as devices continue to get faster, films get thinner and conductors get closer.** Several alternatives exist for replacing conventional CVD dielectrics at the 0.25 micron generation. **The two most commonly used alternatives are high density plasma (HDP) to fill the gaps of tight pitches, and low permittivity materials such as SiOF or Parylene to speed up the device.**

High-density plasma deposition equipment is being used to solve the problem of filling gaps in 0.25 micron lines and spaces. **Fully 54% of roadmaps plan to use HDP deposition equipment for dielectric deposition on 0.25 micron devices**, versus 31% on 0.35 micron devices. High-density plasma deposition equipment can be broken-up by the types of sources being used to generate a plasma. The primary high density sources in use today are helicon wave, ECR, ICP, and TCP. Currently, no single source stands out as having a significant competitive edge over the others. The most experience has been with ECR, and it has had the most development funding.

ECR is a fairly old technology that is just beginning to be applied to CVD for production purposes. **ECR deposition systems have developed a reputation for being able to fill gaps better than do any other systems on the market today. They deposit high quality films that are easy to polish and have lower permittivity than do PECVD deposited films. However, only 8% of those companies planning to use high-density plasma deposition equipment specifically chose ECR equipment. ECR deposited films have tended to be too compressive,**[6] leading to interconnect opens as the film pushes apart underlying aluminum layers. This problem is made worse because ECR deposited films are not self-planarizing. **They need to be polished,** which tends to cause stress fractures in underlying aluminum layers. ECR deposited oxides also **absorb too much moisture.** Unsolved, they must be capped with a PECVD oxide film to prevent moisture absorption. It may be possible to counteract the compressive force of an ECR deposited film with a PECVD deposited film. However, it is not known if this will work. Currently, **these issues are resulting in yield losses. They need to be overcome before ECR deposition equipment can be placed into production.**

Results are less well known about HDP deposition equipment that use other high density sources such as helicon wave, ICP, and TCP. Most of these systems are still in development, so there is little field experience with them. **In comparison to ECR, these systems are relatively simple.** If the lessons learned with HDP etch systems apply to deposition, systems using these other sources should be more reliable than ECR, they should need less floor space, have higher throughput, and have lower cost-of-ownership. However, these are just promises. **These systems are further away from being production worthy than are ECR systems.**

Users are showing reluctance to implement HDP because of its high cost of ownership. The deposition rates of these systems **are**

[6] ECR deposited oxides can have stress that exceeds 200 MegaPascals, almost twice acceptable levels.

typically about 400Å per minute, too slow to be economical. This problem is being solved to some extent with a two-stage process. The first stage uses a 400Å per minute deposition rate while filling fine gaps and then a 4,000Å per minute top coat. This top coat is often deposited in a conventional PECVD or APCVD chamber. This improves the throughput. But it also requires the use of a cluster tool, which adds to system cost. **Overall, throughputs are between 6 and 10 WPH, and system cost is upwards of $3M.** Thus, users still complain of high cost-of-ownership, leading some to look for more conventional alternatives.

Of the companies using CVD equipment without high-density plasma sources, **39% favor conventional TEOS based SiO_2 IMD films**, deposited in either a PECVD or APCVD system.

APCVD deposition of ozone TEOS films is a still potential contender for the inter-metal dielectric market at the 0.25 micron generation. However, these do have significant limitations. **Thick APCVD TEOS films are tensile**, limiting usage in applications above metal films, where they can pull metal lines apart, creating cracks and voids. Many companies have found that in 0.35 micron processes, **this problem could be alleviated by depositing a compressive PECVD SiO_2 layer over the TEOS film**, or by sandwiching the TEOS layer between two PECVD SiO_2 films. Nearly half of the companies in Japan and Korea do this on 0.35 micron processes. While few are confident that this will work on 0.25 micron processes, **it could reemerge as a less expensive alternative to HDP CVD equipment. It might also emerge as a capping step for HDP films.** APCVD ozone TEOS films have the primary advantage of having surfaces that are smooth and are locally planar. In many cases, they do not need to be polished.

PECVD using SiH_4 and H_2O_2 is another alternative that shows promise. Developed by Electrotech, the **APL** (Advanced PLanarizing interlayer-dielectric) **puts down very planar films that do not need CMP.** Mitsubishi has reported that **deep gaps as small as 0.4 micron wide by 0.8 micron can be filled and planarized with this process.** Electrotech claims that 0.2 micron gaps can be filled without any stress problems. However, the film must be capped with a PECVD TEOS to prevent moisture absorption. Also, **reliability issues with this film, and its electrical characteristics are largely unknown since it is so new.**

The need for lower permittivity films has become a significant issue. **Low permittivity films offer significant improvements in device speed.** One of the main advantages of shrinking gate-lengths has been the ever-increasing device speed gained with each shrink. **Device speeds for gate lengths below 0.35 micron will be limited unless the dielectric constants of interlayer insulators are lowered.** This is because the spaces between conductors are scaled with linewidths. As this happens, inter-metal dielectrics sandwiched between two conducting lines can become so thin that capacitive coupling slows the device excessively, or cross-talk creates errors. Lowering the dielectric constant solves this problem and enhances the speed of the device.

The maximum frequency at which a chip can operate is mostly limited by delays in the interconnect wiring. This is often referred to as the RC delay (R for resistance and C for capacitance). An electrical circuit derivation showing how this occurs is

given in presentation 8. Time delay is a function of the length and width of the conductors, the distance between conductors, the resistivity of the conductor materials and the capacitance of the dielectric materials separating them.

The easiest way to make a circuit run faster is to lower time delay by making conductors shorter or narrower or by increasing the separation between the conductors. Making conductors shorter and narrower is essentially what is done when a chip maker scales a design to a lower linewidth. Reducing linewidths has many other benefits as well. This is the fundamental driver that makes Moore's law work. Conductors can also be made shorter, with wider spaces by adding global interconnect layers. But this is expensive. So, increasing the separation between conductors is something no chip manufacturer likes to do.

The only **alternatives are to lower resistivity, to lower permittivity, or to do both. Resistivity can be lowered by replacing aluminum interconnect films with copper. Permittivity can be lowered by making SiO_2 less dense, or by replacing it with new materials that have a lower dielectric constant**. This is why there is so much the interest in new materials for deposition and why there are so many opportunities for both chip makers and equipment makers.

Most semiconductor companies want IMD films with a relative dielectric constant of 3.0 or below for 0.25 micron processes. Companies are exploring several new dielectric materials for intermetal dielectric films in order. This includes modifying SiO_2 by adding fluorine and by using entirely new materials such as organic polymers (see presentation 9).

Organic polymers generally offer the lowest dielectric constants, and have excellent gap-filling ability. Spin-on-dielectrics also offer the advantage of low temperature deposition, equipment costs are a third that of HDP systems, and throughputs are four times greater. However, some organic polymers such as BCB and Teflon are soft, and so aluminum hillocks can easily penetrate them, causing shorts. They are also more susceptible to electromigration problems. Spin-on-Dielectrics (SOD) that are not soft must be cured at high temperatures. For example, spin-on-glass needs to be cured at 600°C.

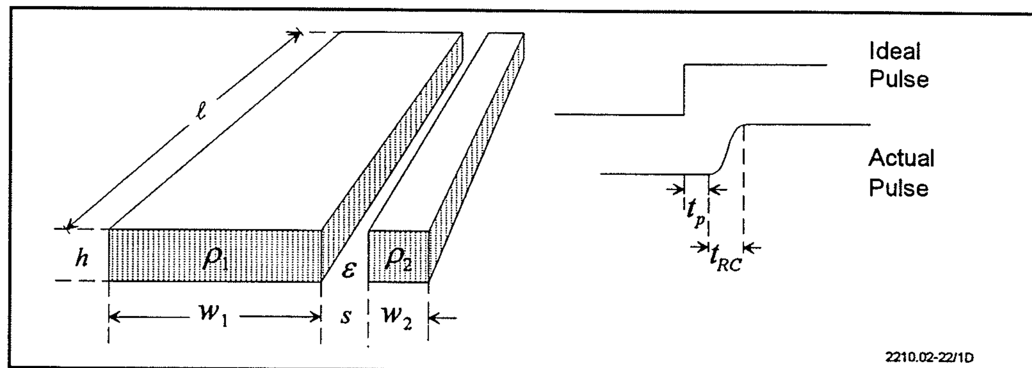
Overall, each type of organic polymer has one or more problems with out-gassing, high thermal coefficients of expansion, plasma-etch resistance, thermal stability, via poisoning, water absorption, and adhesion. These issues are especially true for dielectrics that are spun-on. **These problems are fundamental reliability barriers that must be overcome before such films can be used in production**. *If this can be accomplished, they would be a substantial threat to CVD because of their lower cost-of-ownership.*

Some companies work around these problems by capping the organic film with an inorganic film. This has worked successfully with spin-on-glass (SOG) and is used in production today. It has also been done with parylene in an R&D environment. Parylene was only used to fill the gaps between metal lines. The parylene was then coated with a low temperature oxide film. It works, but it is expensive. Deposition rates for Parylene range from 100 to 400Å per minute.

Presentation 8

How Resistivity and Permittivity Affect Device Speed

(on a single conducting layer)



As a Lumped Sum Model:

Time Delay = $t_{RC} = (R_1 + R_2)C \Longrightarrow$ (R_1, R_2, C)

Where t_p = Propagation Delay
t_{RC} = RC Time Constant
R = Resistance
C = Capacitance
ρ = Resistivity
ε = Dielectric Constant (Permittivity)

$$= t_{RC} = \left[\frac{\rho_1 \ell}{h \bullet w_1} + \frac{\rho_2 \ell}{h \bullet w_2}\right] \bullet \frac{\varepsilon \bullet h \bullet \ell}{s}$$

Assume $\rho_1 = \rho_2 = \rho$

$$= \rho \bullet \varepsilon \left[\frac{1}{w_1} + \frac{1}{w_2}\right] \bullet \frac{\cancel{h} \bullet \ell^2}{\cancel{h} \bullet s}$$

let $w_1 = K_1 \bullet w_2$ $\quad$ K_1 = Relative Conductor Width

let $s = K_2 \bullet w_2$ $\quad$ K_2 = Relative Separation

$$= \rho \bullet \varepsilon \left[\frac{1}{K_1 \bullet w_2} + \frac{1}{w_2}\right] \frac{\ell^2}{K_2 \bullet w_2}$$

$$= \rho \bullet \varepsilon \left[1 + \frac{1}{K_1}\right] \frac{\ell^2}{K_2 \bullet w^2}$$

Therefore to Go Faster:

- Make the conductors shorter or narrower (ℓ or w),
- Increase the separation between conductors (K_2),
- Decrease permittivity (ε),
- Decrease resistivity (ρ) or,
- A combination of the above.

Source: VLSI RESEARCH INC
2210.02-22/2M

Presentation 9

IMD Dielectric Film Alternatives

Material	*Dielectric Constant*	*Type*	*Process*
SiO_2	4.2–4.8	Inorganic	PECVD
SiO_2	3.9–4.1	Inorganic	O_3TEOS Sandwich
SiO_2	3.6–4.2	Inorganic	ECR
SiOFx	3.0–4.0	Inorganic	PECVD
HMCTZ[1]	3.1	Organic	PECVD
Polyimide	3.0–3.7	Organic	Spin-On
BCB[2]	2.6	Organic	Spin-On
Parylene	2.4	Organic	PECVD
Teflon AF	1.9–2.0	Organic	Spin-On
Aerogel	1.1–2.0	Inorganic	Spin-On

[1] *Hexa-Methyl-Cyclo-TrisilaZane*
[2] *Benzo-Cyclo-Butenes*

Source: Dow Chemical, Motorola, Nanopore, SEMATECH, Nikkei Microdevices and Texas Instruments.
2210.02-7P

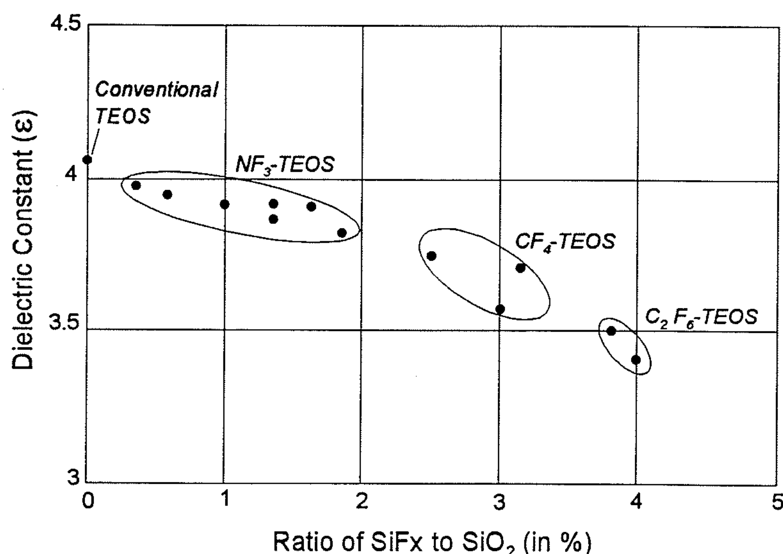
There are several reasons that **lead us to believe that organic films, and SODs in particular, will not have a significant effect on the deposition equipment market in the near term.** These are: Major break-throughs are needed to make them viable for production. Organic materials have a poor track record of being able to deliver on promises over the past ten years. Chip makers are always reticent to change materials.

One of the most telling signs about the near term future of organics is that they did not show up in our compilation of roadmaps. They remain mired in research.

The most viable low permittivity alternative for IMD films seems to be with the addition of fluorine to SiO_2 films. Motorola and others have reported SiOF films with relative dielectric constants as low as 3.0. **Some have used APCVD TEOS and C_2F_6 to achieve a relative dielectric constant of 3.4 with a 4% silicon-fluorine concentration** (see presentation 10). **SiOF films also have low stress.** The use of fluorine has not proven to be a problem because it is sufficiently well removed from junctions and barrier metals to prevent its migration. However, these films have had stochiometry problems as well as moisture and carbon contamination. Watkins-Johnson has used

Presentation 10

Fluorine Lowers Permittivity in SiO_2 Films



Source: Nikkei Microdevices
2210.02-8D

HDPCVD to deposit SiOF film with low moisture absorption and good stochiometry. **There is an opportunity for CVD equipment makers to provide systems that can deposit films with uniform distributions of fluorine and with low contamination.**

ECR CVD offers another important alternative for reducing the relative dielectric constant. It **can lower the dielectric constant of SiO_2 films from 4.1 to 3.6 by depositing less dense films**. However, ECR CVD deposited films have several problems that need to be overcome before being used in production. Foremost is the previously-mentioned stress problem. Stress might be controlled by capping the film with a tensile film layer. Another issue is moisture absorption, which also needs to be controlled by depositing an additional film. At least one company has been able to achieve the same level of moisture resistance with ECR as with traditional plasma CVD SiO_2. This company deposited a SiON film to cap the ECR layer. However, these additional steps only serve to make ECR more expensive.

Another approach may be the use of Aerogel, a new material developed by NanoPore in conjunction with Texas Instruments. Aerogel is a porous silicon dioxide film. It has thermal stability to 900°C and the dielectric constant can be tuned to user needs. However, it has very low thermal conductivity. So heat dissipation will be a problem to overcome with this film. Additionally, Aerogels have low mechanical strength and they are unproven in semiconductor manufacturing.

One of the most elegant approaches would be to use air as a dielectric. This is already done by GaAs chip makers. They call this 'air bridging.' However, the high interconnect density, large chip sizes, electromigration problems, and high tensile stress of aluminum in CMOS circuits will probably prevent the use of air bridges.

Currently, there are few good solutions to the permittivity issue. This presents a tremendous opportunity for equipment companies that can provide solutions. Dielectric constants near or below 3.0 will likely prove difficult to achieve in 0.25 micron processes. **It** is, however, **likely that the industry will achieve 3.5 epsilon with 0.25 micron processes. Equipment companies should expect customers to demand this to become a moving target, with roughly a 0.5 drop in relative dielectric constant for each new generation of device for the foreseeable future.**

Plugs & Interconnect

The thin films used for interconnects in 0.25 micron processes are essentially the same as that for 0.35 micron processes: titanium-nitride(TiN), tungsten(W), and aluminum alloys(AlCu and AlCuSi). **Copper is the only deviation from this, and it is in the 0.25 micron roadmap of only a small portion of chip makers (15%).**

TiN films are used by all companies in contacts and by 69% of companies in vias. It is essential in contacts[7] as a barrier to prevent spiking. It is also used in vias[8] and on dielectric surfaces to provide adhesion be-

[7] Contacts are the windows through which the first level metal connects to the source and drain junctions.

[8] Vias are the windows through which metal layers interconnect with each other.

tween aluminum and oxide layers. Finally, it can be deposited after aluminum as an anti-reflective coating to reduce alignment errors in steppers. TiN films are almost universally sputtered in 0.35 micron processes.

CVD of TiN films overtakes sputtering at the 0.25 micron node of the roadmap. As contacts and vias get deeper and narrower, sputtering of TiN films can leave the lower corners of contacts open to spiking. This can leave bulges at the top corners which shadow later deposition steps (see presentation 11). CVD is more conformal and less expensive than sputtering. However, **readers should be cautious, as CVD equipment for TiN films has been one of those technologies that has kept getting pushed out with each new generation.** Two years ago, 22% of 0.35 micron processes had it designed-in; currently, only 8% have it designed-in for this generation. **CVD-deposited TiN films have a reputation for being prone to contamination and uniformity problems.**

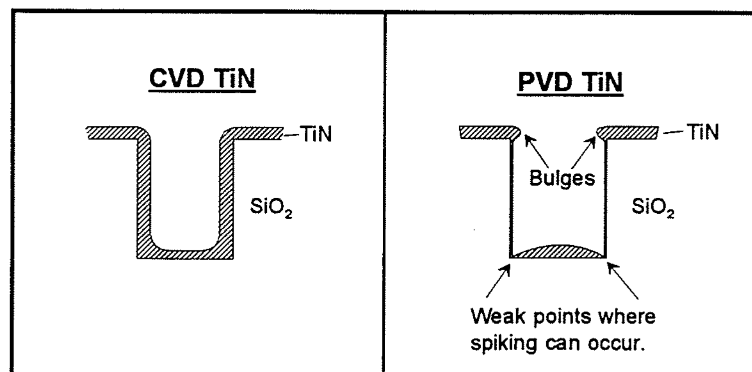
The use of tungsten to fill plugs is one of the most controversial topics in the industry. It is used by some to fill contacts and vias, while others get by with only reflowed aluminum alloy deposition. Logic circuit manufacturers and captive manufacturers tend to be among the first group; memory manufacturers tend to be among the latter. This occurs largely because memories have fewer metal layers, the dielectrics are thinner, and aspect ratios are lower. Moreover, fewer metal layers alleviate concerns about the thermal cycling needed to reflow aluminum at each interconnect layer, and concerns about how it might damage previously deposited aluminum layers.

Tungsten plugs offer the easiest and fastest way to achieve multi-level metal, especially true when aspect ratios are above three-to-one. However, they are the more costly approach. The incentive for eliminating tungsten plugs is simple: substituting an aluminum alloy plug can save over $15 per plug layer. Obviously, control of the sputtering process is the key to eliminating tungsten plugs.

Two primary methods are used for filling plugs with aluminum: that of controlling the delivery mechanism, and that of controlling the surface mobility of aluminum at the wafer's surface. With conventional sputtering, particles that leave the target at high incident angles get caught on the upper corners of windows (see the top box of presentation 12). The build-up eventually closes off the tops of the windows, leaving an open "keyhole" (see presentation 13). Keyholes are a reliability problem, at a minimum. At worst, they form voids be-

Presentation 11

CVD Versus PVD for Titanium-Nitride Contact Barriers



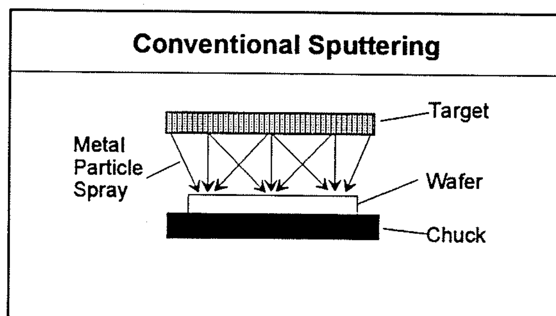
Source: VLSI RESEARCH INC
2210.02-9D

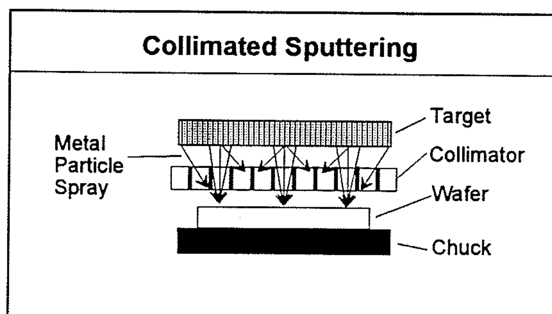
tween the upper metal level and lower contact point, creating shorts. Then the device may not function at all.

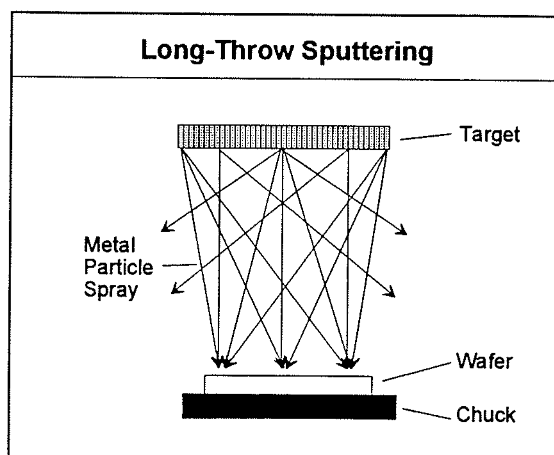
This particular problem was largely solved by Varian in the early nineties. Introducing **collimated sputtering**, Varian put a honeycomb screen[9] between target and wafer (see the center box of presentation 12).

Presentation 12

Sputtering Delivery Methods







Source: VLSI RESEARCH INC
2210.02-10D

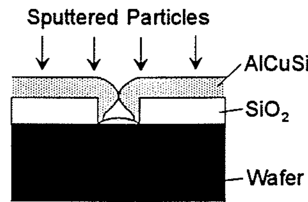
High angle particles of aluminum are caught by the honeycomb, while low angle particles travel directly at the wafer, providing better filling of windows without keyholes. There are some disadvantages to this approach: it is slower because fewer particles arrive at the wafer's surface; deposition rates slow as the collimator captures particles and its walls thicken; and there is a constant contamination worry from the collimator itself. Nevertheless, these issues have been largely dealt with, and now **collimated sputtering is a mainstream technology in production use by many manufacturers today.**

Long-throw sputtering was recently introduced to provide greater advantages over conventional sputtering without the need for a collimator. High-angle particles are dealt with by pulling the target away to a position that is roughly 12 inches from the chuck. In this manner, they harmlessly fly out to a process chamber liner for easy cleaning. **Long-throw sputtering promises to provide lower particulate contamination than do collimators, as well as a constant deposition rate. Its primary disadvantage is** that high-angle particles from one end of the target can adhere to the upper corners of windows on the far side of the wafer, **causing lop-sided keyholes at the outside of the wafer.** Possibly compounding this problem is a **resulting reduction in thickness uniformity. The films can become dish-like.** Another complication is that process chambers must be larger to account for the long-throw. It is too early to say whether this technique will become as mainstream as collimated sputtering. Our sense is that the benefits are small, and do not outweigh the disadvantages.

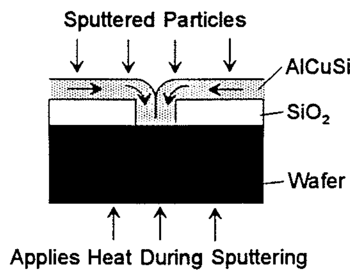
[9] Called a collimator.

Evolution of Sputtering Techniques for Plug Filling

Conventional Sputtering: ***results in keyholes . . .***

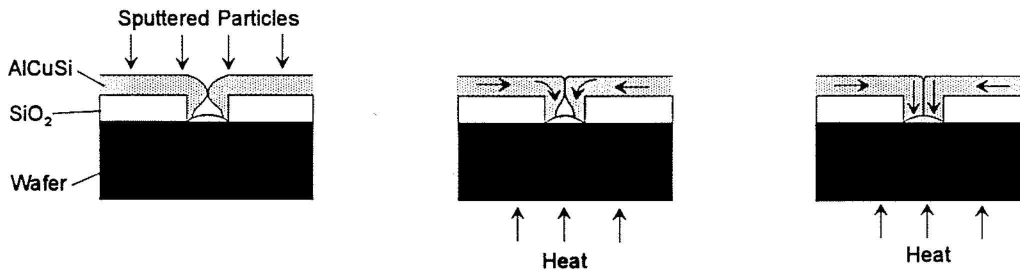


Hot Sputtering: ***using high temperature helps flow aluminum into the plug . . .***



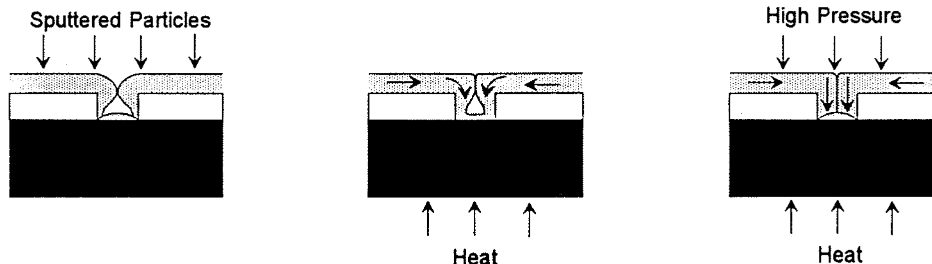
. . . but the surface is not planar.

Reflow Sputtering: ***using high temperature after sputtering provides better planarity . . .***



. . . but temperatures exceed 500° C.

High Pressure Sputtering: ***forces hot metal into the gap . . .***



. . . lowers process temperatures to 400° C.

Source: VLSI RESEARCH INC
2210.02-11D

Using a collimator or long-throw sputtering system is seldom enough to fill deep plugs. Metal must be made to flow into the gaps. Controlling the surface mobility of aluminum at the wafer's surface is done primarily by heating the wafer to cause aluminum to flow into plug gaps (see presentation 13). Hot sputtering is the oldest plug-filling technique. It is seldom used because of uniformity and resistivity issues. **Reflow sputtering** is the most common technique. **It is used in almost all 0.35 and 0.25 processes where aluminum is used to fill plugs.** Reflow sputtering is a multi-step process which requires a cluster tool. Aluminum is first deposited, then reflowed in a separate chamber. The metal literally flows into the gap. **This technique, combined with a collimator, works well through 0.25 geometries and aspect ratios of 3-to-1.** The disadvantage of this technique is that it requires process temperatures above 500°C. This can damage underlying metal layers and cause junctions to move.

Metal layers are becoming very sensitive to thermal cycling. Opens and microcracks in global interconnect have become the leading source of yield loss. AlCuSi films that are adhered to a SiO_2 film can exhibit several hundreds of megapascals tensile stress at room temperature. Small vacancies in the AlCuSi can coalesce to form voids in the interconnect as the device is thermally cycled.

High-pressure (HP) sputtering is a new technique, developed by Texas Instruments, Mitsubishi, and Electrotech **to lower the deposition temperature needed for reflow sputtering**. It uses a combination of heat and pressure to extrude the aluminum into plug gaps, overcoming any surface tension issues. **It** also **lowers the maximum chamber temperature needed to induce reflow, to 400°C. As a result, it can fill 4-to-1 aspect ratios, which could push it well beyond 0.25 micron gaps.** Its primary disadvantage is the fear instilled by the use of high pressures. **In some areas, safety laws have prevented its introduction.** If this problem can be overcome, high-pressure sputtering can be expected to have a healthy future in the industry.

The move to AlCu from AlCuSi is another significant trend. Fully 54% of roadmaps have AlCu as the material for forming global interconnect wiring. Silicon is no longer needed in AlCu films to prevent spiking because of TiN barrier metals. Some users have found that silicon was not really needed to stuff grain boundaries in order to prevent electromigration. At worst, there is only a minor loss of electromigration resistance.

Copper interconnect is another conspicuous trend in the selection of metal for 0.25 micron processes. Most agree that copper interconnect will play a significant role in some future device generation. Fully 15% of roadmaps currently have it designed-in for 0.25 micron processes. **Copper is not expected to become prevalent in this process generation** because deposition equipment is not readily available, and because it can't yet be etched. Using copper requires a damascene process. Moreover, **the benefits that copper provides in low resistivity do not appear to be worth the effort to bring it into production**. Copper is only 70% more conductive than is aluminum. It makes much more sense to focus research efforts on low permittivity dielectrics.

CMP

Chemical mechanical planarization is expected to play a more prominent role in 0.25 micron processes. All of the major chip makers have research programs in CMP. A few have it in production for 0.6 micron multi-level processes, roughly one-third have it in 0.35 micron processes, and over half plan to use it in 0.25 micron processes.

CMP can be used twice in the first metal film stack and twice in each film stack thereafter. It is used extensively by microprocessor manufacturers, as they have the most complex metallization. It is used sparingly by ASSP and SRAM producers. The general view is that American companies are in the lead in adopting CMP, while Asian companies have been playing catch-up. However, many Asian companies take a different view of this. They believe that the use of tungsten plugs and CMP is a sign of technical weakness. Nevertheless, they are working hard to develop CMP processes. No one disagrees with the belief that CMP will play a key role in future manufacturing strategies. **How and when it is implemented will make significant differences in a company's cost structure, as well as a new design's success in the market**.

The use of CMP for the pre-metal-dielectric accounts for a large part of its application. **The PMD layer was one of the first films to be CMP'd. However, it no longer accounts for the largest part of applications.**

Chip makers are using CMP on inter-metal dielectrics more than with any other film. This is being done on unpatterned dielectrics and ones with tungsten plugs. The reason for this is that **there are few good alternatives for planarization *after* the PMD layer. None will provide planarization as good as does CMP.**

The range of IMD films that can be used are limited by other film requirements, such as low stress and dielectric constant. The use of ozone TEOS precursers planarizes SiO_2 films, but it produces too much stress. While the stress can be alleviated with additional PECVD layers, the dielectric constant may be too high. PECVD with etchback provides insufficient planarization below 0.5 micron; SOD[10] is too unstable for production; HDP CVD produces triangular projections which must be polished away. All of these factors make CMP the quickest and easiest way to achieve multi-level metallization.

The use of CMP on blanket tungsten is already favored over etchback for 0.35 micron processes and this is expected to grow in the transition to 0.25 micron processes. Tungsten etchback has never worked well, as it leaves contamination in the dielectric film as well as on the surface. This affects both yield and reliability. Cleaning etch-backed tungsten is problematic because there are stringers on the surface that are difficult to remove using wet chemistries. Moreover, it is impossible to finish with flat plug surfaces using etchback. Facets or mushroom caps are usually left at the plug sites. These have a negative effect on yield. There are also difficulties with plasma etching at the interface edges, where tungsten and oxide meet on the surface of the wafer. This can create voids, which affect the reliability of the devices. CMP solves these because it not only flattens the wafer, it also removes all stringers and surface contamination in the film.

---

[10] Spin-On-Dielectric.

While CMP offers many benefits, its primary disadvantage is cost. This has lead many manufacturers to find ways to design it out of processes as more experience is gained. **Plans for using CMP for 0.35 micron devices have dropped significantly in comparison with those from a similar survey two years ago** (see presentation 14). These changes have been significant enough to slow the growth of the CMP equipment market.

Passivation

Passivation is normally an area where little technical change occurs. However, in the jump to 0.25 micron films, some companies have expressed a need for low dielectric constant films at this step as well (see presentation 15). In general, there will be a trend toward less silicon-nitride and more silicon-dioxide films using TEOS chemistries. There is also some interest in using high density PECVD at this step. However, we doubt that the cost justifies the benefits at this normally non-critical step.

– G. Dan Hutcheson
– Jiong Chen, Ph. D

Presentation 14

Trends in 0.35 Micron BEOL Roadmaps
(a comparison of views over two years)

	Industry Usage Plans as Stated in . . .		
	1993	***1995***	***Trend***
Metal Interconnect:			
AlSi	61%	0%	↓
AlCu	0%	42%	↑
AlCuSi	39%	46%	↗
Tungsten	6%	4%	↘
Tungsten Plug	50%	54%	→
CVD TiN	22%	8%	↘
Planarization:			
CMP	81%	52%	↘
Damascene	13%	0%	↓
SOD	6%	0%	↓
Undecided	13%	0%	↓

Source: VLSI RESEARCH INC
2210.02-12D

Presentation 15

Passivation Trends
(usage in percent†)

Layer	*Process*	*LINEWIDTH* 0.35µm (%)	*LINEWIDTH* 0.25µm (%)
Passivation	PECVD SiN	62	46
	HD PECVD SiN	0	8
	PECVD TEOS	8	0
	Low ε PECVD TEOS	0	15
	PECVD SiO_2	31	38

†*Totals may add to greater than 100% because of multifilm sandwiches.*

Source: VLSI RESEARCH INC
2210.02-13P

Background Material

- Glossary of deposition terminology.
- Guide to thin films.
- How resistivity and permittivity affect device speed.

Glossary of Deposition Terminology

Adhesion Layer: Films used to make aluminum alloys stick to underlying dielectrics and vice-versa. In the latter use, they are called Anti-Reflective-Coatings (ARC) by lithographers. The most common adhesion layer is titanium-nitride (TiN) which is also used as a barrier layer.

APCVD: Atmospheric Pressure Chemical Vapor Deposition.

Barrier: Films used to provide a barrier between aluminum metal films and junctions. The barrier prevents aluminum from growing spikes into the silicon that penetrate and short circuit the underlying junction, thereby degrading device performance. The most common barrier in use is titanium-nitride (TiN), which is also used as an adhesion layer.

BEOL: Back-End-Of-the-Line, processes are used to form the global interconnection of circuit elements. It comprises all wafer process steps after the last local interconnect layer in wafer fabrication. The primary purpose of BEOL processes are to wire together all the transistors put down in FEOL (Front-End-Of-the-Line) processes. Not to be confused with the term "back-end," which refers to test and assembly.

CMP: Chemical-Mechanical-Planarization levels the surface of the wafer using a polisher.

Dielectric Constant: From The New IEEE Standard Dictionary of Electrical and Electronic Terms, "The property which determines the electrostatic energy stored per unit volume for unit potential gradient." It is represented by the symbol ε or k, when it is measured as a relative value to that of a vacuum or air.

ε : The Greek symbol used to represent the relative dielectric constant.

FEOL: Front-End-Of-the-Line, comprises all wafer process steps starting from when the wafer starts into production until the last local interconnect layer. Not to be confused with the term "front-end," which refers to all of wafer process.

Film Sandwich: A set of films deposited sequentially without a masking or etching. When completed, the set serves the function of one film. It can be an insulator or conductor. Film sandwiches are used when material limitations require other, offsetting materials. For example, when the high stress films like ozone TEOS or ECR deposited SiO_2 limit their use over aluminum.

Film Stack: The set of films needed to complete one interconnection layer. This includes the dielectric film used to isolate the metal film from lower conductors, the barrier metal plugs, and the conductor metal. It differs from a film sandwich in that mask steps separate the layers and both conductive and insulating film layers are used.

Global Interconnect: Conductive film layers that are used in the BEOL to make the wiring that connect circuits across the entire chip, hence the term "global." These films must have low resistivity in order to conduct signals long distances without losing them. Consequently, they are always composed of metals such as aluminum, tungsten, or copper. See local interconnect.

HDP: High Density Plasmas have electron densities of 10E17 or higher. This density is two-to-three orders of magnitude above that of normal plasmas. Typical sources which provide high density plasmas are ECR (Electron Cyclotron Resonance), Helicon wave, ICP (Inductively Coupled Plasma), TCP (Transformer Coupled Plasma), and HRe (High density Reflected electron).

ILD: Inter-Layer Dielectrics are insulating films which are placed between conductive films. They are used throughout the process. For BEOL applications, this includes both IMD and PMD films. ILD films are also used in FEOL applications for insulating films placed between polysilicon films or between polysilicon and the silicon substrate. These dielectric films are used to cover gates, to cover bit lines, to cover resistors, and to make capacitors. The term ILD has become somewhat redundant because it can be used to describe all of the dielectric layers except passivation.

IMD: Inter-Metal Dielectrics are insulating films which are placed between metal interconnect levels.

Local Interconnect: Conductive film layers that are used in the FEOL to "strap" together circuit elements such as transistors, resistors and capacitors to each other and to global interconnect layers, hence the term "local." These films do not need the low resistivity of global interconnect layers. But they must be able to withstand the high temperatures used in FEOL processes. See global interconnect.

MPIL: Mask-Per-Interconnect-Level is the average number of masks needed to complete a metal interconnect layer. It is a measure of manufacturing efficiency in semiconductor processes. Lower MPIL numbers result in greater manufacturing efficiency and lower cost.

Passivation: A sealing layer added at the end of the fabrication process to prevent deterioration of electronic properties through chemical action, corrosion, or handling during the packaging process.

PECVD: Plasma Enhanced Chemical Vapor Deposition.

Permittivity: From The New IEEE Standard Dictionary of Electrical and Electronic Terms, "The change in electric displacement per unit electric field when the magnitude of the measuring field is very small compared to the coercive electric field." Relative permittivity is synonymous with "relative dielectric constant."

PMD: Pre-Metal-Dielectric is the dielectric film used to insulate the last FEOL conductive film from the first BEOL global interconnect film. The last FEOL conductive film is usually made of polysilicon. It is occasionally made of other materials such as tungsten-silicide and tantalum-silicide. This is a term that emerged as a result of the need to distinguish it from inter-metal dielectrics.

SOD: Spin-On-Dielectrics include dielectric materials that can be deposited using a spinner. These materials include SOGs (Spin-On-Glass), Polyimides, BCBs (Benzo-Cyclo-Butenes), Teflon and Aerogels.

TEOS: Tetra-Ethyl-Ortho-Silicate is a precursor material used to form SiO_2 films.

Presentation 16

A GUIDE TO SEMICONDUCTOR FILMS

Line Location	WHAT THE FILM IS: Purpose	WHAT THE FILM IS: Composition	CHARACTERISTICS 1	CHARACTERISTICS 2	WHAT THE FILM DOES 1	WHAT THE FILM DOES 2	DISADVANTAGES 1	DISADVANTAGES 2	Process Location	COMMON CATEGORIES: Equipment	COMMON CATEGORIES: FAB
BEOL	Conductor	Al Alloys	good restvt.	Low Temp	Global Intrcnct		Poor plug fill		Uppermost metal lyrs	PVD	Metalization
		Al Alloys	good restvt.	HI Temp	Global Intrcnct	Good plug fill	Hi-temp reflow		Uppermost metal lyrs	Reflow PVD	Metalization
		Al Alloys	good restvt.	Low Temp	Global Intrcnct	Best Al plug fill	Unprvn tech.		Uppermost metal lyrs	Hi Press PVD	Metalization
		Cu	Exel. restvt.	Res elctrmgrtn	Global Intrcnct		Unprvn tech.	Not etchable	Uppermost metal lyrs	MOCVD	Metalization
		TiN	good restvt.	Low Temp	Barrier	Adhesion layer			Contact & vias	PVD	Metalization
		TiN	good restvt.	Excl stp covrg	Barrier	Adhesion layer	Reprodcablty		Contact & vias	LPCVD	Deposition
		W, Blanket	Mod. restvt.		Global Intrcnct				Metal, 1st	LPCVD	Deposition
		W, Blanket	Mod. restvt.		Best Plug fill		COO		Contact & vias	LPCVD	Deposition
		W, Selective	Mod. restvt.		Best Plug fill		Reprodcablty	COO	Contact & vias	LPCVD	Deposition
	Insulator	BCB	Lo permittivity	Organic SOD	Lo permittivity	Gap fill	Outgassing	Spiking	IMD	Spinner	Deposition
		BPSG/O3 TEOS	Low temp.	Surfc leveler	Gap fill	Etch Selectivity	Stress	PECVD sand.	IMD/ILD	APCVD	Deposition
		BPSG/PSG	Low temp.	Surfc leveler	Isolates	Etch Selectivity	Hi-temp reflow		ILD/Passivation	PE/APCVD	Deposition
		BPSG/TEOS	Low temp.	Surfc leveler	Isolates	Planarizes	Etchback	COO	IMD	PECVD	Deposition
		HMCTZ	Lo permittivity	Organic	Lo permittivity	Gap fill	Unprvn tech.	COO	IMD	HD PECVD	Deposition
		Parylene	Lo permittivity	Organic	Lo permittivity	Gap fill	Outgassing	Stress	IMD	PECVD	Deposition
		Si3N4	High Purity	Trnsmt light	EPROM prog.	preservative	Cracks	Req. SiO2 lyr	Passivation	PECVD	Deposition
		Si3N4	Low temp.		preservative		Cracks	Req. SiO2 lyr	Passivation	PECVD	Deposition
		SiO2	Low temp.		ILD		Req. CMP	COO	IMD	AP/PECVD	Deposition
		SiO2	Low temp.		ILD	Gap fill	Strs W/ECR	Req. CMP	IMD	HD PECVD	Deposition
		SiOFx	Lo permittivity	Low temp.	Lo permittivity	ILD	Strs W/ECR	Req. CMP	IMD	HD PECVD	Deposition
		Teflon	Lo permittivity	Organic SOD	Lo permittivity	Gap fill	Outgassing	Spiking	IMD	Spinner	Deposition
	Sacrifical	Si3N4	lo qual. isoltn		Etch Mask		Cracks		Over films.	PECVD	Deposition
		SiO2	lo qual. isoltn		Etch Mask				Over films.	AP/PECVD	Deposition
		SOG	Organic SOD	Soft	Planarizes		Outgassing	Spiking	Over conductors	Spinner	Deposition
FEOL	Conductor	MoSi Silicide	intrfce mitigtr	Self-aligning	Contact integrt.		COO		Ovr gte, junc, & loc int.	PVD	Metalization
		Platinum	good restvt.	Low Temp	Capacitor plate		COO		Capacitor plate	PVD	Metalization
		Poly silicon	poor resistvt.	Hi temp.	Capacitor Plate				Capacitor	LPCVD	Deposition
		Poly silicon	poor resistvt.	Hi temp.	Gate conductor				Gate	LPCVD	Deposition
		Poly silicon	poor resistvt.	Hi temp.	Bit/word lines	Resistors	poor resistvt.		Local interconnect	LPCVD	Deposition
		TaSi Silicide	intrfce mitigtr	Self-aligning	Contact integrt.		COO		Ovr gte, junc, & loc int.	PVD	Metalization
		W polycide	poor resistvt.	Hi temp.	Straps		poor resistvt.		Local interconnect	LPCVD	Deposition
		WSi Silicide	intrfce mitigtr	Inexpensive	Contact integrt.				Ovr gte & loc int.	LPCVD	Deposition
	Insulator	BPSG/O3 TEOS	Low temp.		Isolates	Planarizes	Stress		ILD	APCVD	Deposition
		BPSG/TEOS	Low temp.		Isolates	Planarizes	Etchback	COO	ILD	PECVD	Deposition
		BST	Hi permittivity	Dense	Hi qual. Dielec.	SiO2 replcmnt	Uniformity	Stability	Gate insulator	MOCVD/PVD	Deposition
		SiO2	Low temp.	Low COO	Isolates	ILD/Isolatn fill	Contaminants		Betwn trans, Int-poly	APCVD	Deposition
		SiO2	Low temp.		Isolates	ILD/Isolatn fill			Betwn trans, Int-poly	PECVD	Deposition
		SiO2	Mod temp.		Isolates	ILD/Isolatn fill	Mod temp.		Betwn trans, Int-poly	LPCVD	Deposition
		SiO2	Hi permittivity	Dense	Charge Stor.		Hi temp.		Capacitor dielectric	Furnace/RTP	Diffusion
		SiO2	Hi permittivity	Dense	Hi qual. Dielec.		Hi temp.		Gate insulator	Furnace/RTP	Diffusion
		Tantalum Pentoxide	Hi permittivity		Charge Stor.		Stability	Reliability	Capacitor dielectric	PECVD	Deposition
	Sacrifical	Si3N4	lo qual. isoltn		Etch Mask		Cracks		Over films.	PECVD	Deposition
		Si3N4	lo qual. isoltn		Implant Barrier		Cracks		Over substrate	PECVD	Deposition
		SiO2	lo qual. isoltn		Etch Mask				Over films.	AP/PECVD	Deposition
		SiO2	lo qual. isoltn		Implant Barrier				Over substrate	AP/PECVD	Deposition
		SOG	Surfc leveler	Organic SOD	Planarizes		Outgassing	Spiking	Over conductors	Spinner	Deposition
	Spacer	Si3N4	lo qual. isoltn		Ldd Drain				Gate, Sidewall	PECVD	Deposition
		SiO2	lo qual. isoltn		Ldd Drain				Gate, Sidewall	AP/PECVD	Deposition
	Semiconductor	Epitaxial Silicon	Hi qual. layer		Prev. latch-up	Defct free surf.	COO		Substrate	Epi Reactor	Wafer Supplier

Source: VLSI RESEARCH INC
2210.02-19XLS

Presentation 17

How Resistivity and Permittivity Affect Device Speed

(between conducting layers)

$$t_{RC} = t_2 - t_1 = (R_1 + R_2) \bullet C \quad \text{(as a lumped sum model)}$$

Where: t = time
R = Resistance
C = Capacitance

$$= \left[\left(\frac{\rho_1 \bullet \ell}{w \bullet T_{f1}}\right) + \left(\frac{\rho_2 \bullet \ell}{w \bullet T_{f2}}\right)\right] \bullet \frac{\varepsilon \bullet w \bullet \ell}{T_D}$$

Where: ρ = Resistivity
ε = Dielectric Constant

$$= \left[\frac{\ell^2 w}{w\, T_D}\right]\left[\varepsilon \left\{\frac{\rho_1}{T_{f1}} + \frac{\rho_2}{T_{f2}}\right\}\right]$$

let $T_{f2} = K_1 \bullet T_{f1}$, $0 \le K_1 \le \infty$ (a parameter)

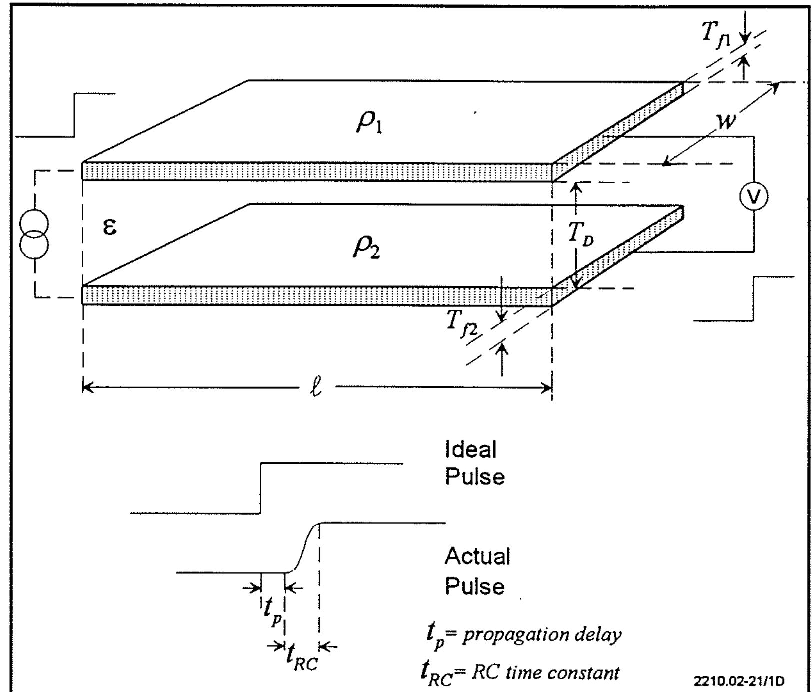
$$= \frac{\ell^2}{T_D \bullet T_{f1}}\left[\varepsilon \left(\frac{\rho_1}{1} + \frac{\rho_2}{K_1}\right)\right]$$

let $\rho_2 = K_2 \bullet \rho_1$, $0 \le K_2 \le \infty$

$$= \left[\frac{\ell^2}{T_D \bullet T_{f1}}\right]\left[\varepsilon \bullet \rho\right]\left[1 + \frac{K_2}{K_1}\right]$$

Assume $K_1 = K_2 = 1$

$$t_{RC} = \frac{2\ell^2}{T_D \bullet T_{f1}}(\varepsilon \bullet \rho)$$



a) time delay increases with square of the length
b) time delay decreases with dielectric thickness or thin film thickness
c) time delay increases with ε and ρ

Therefore To Go Faster:

- Make It Thinner, Shorter, Or Thicker,
- Or Decrease Epsilon (ε),
- Or Decrease Resistivity (ρ),
- Or A Combination Of All Of The Above.

Source: VLSI RESEARCH INC
2210.02-21/2M

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