The Chip Insider®

***February 5, 2010 – From the Front Lines**: Multi-Pattern Technology Economics and Killer Defect Economics.*

Multi-Pattern Technology Economics: Also known as DPT, or dual pattern technology, it struck me as odd that many continue to use conventional, CoO to analyze its value. It's really a misapplication of CoO, because CoO was designed to compare tools on raw cost, not to make economic decisions about process flows. So let's go back to basics: MPT cost analysis needs to start with the following variables:

MPT Cost = f(N, S, K, M, L, …)

Where:

- N = Number of exposures per mask
- S = Shrink
- K = Additional cost per wafer due to the shrink
- M = Critical Share of total litho cost
- L = Litho Share of total wafer cost

Now if the other variables beyond this are constant, and they are in this instance, then at a basic level

$$\text{MPT Cost} = 1 - S^2/N$$

So, if we add an exposure, and we have a linear shrink to 70%, then the gain from the shrink is only 2%. Chip makers have always feared multiple exposures because of this. But in reality this level of analysis only factors the cost per layer. So let's factor in the entire process:

$$\text{MPT Advantage per Wafer} = 1 - K*(L*M*S^2/N + S^2*(1-L*M))$$

So, if L = 0.35, M = 0.40, and K = 1.30, then the cost gain from using a DPT litho strategy becomes 45%. That's why it makes sense. Admittedly, the values I have chosen are just in the ballpark and you need to you your own assessment with your own numbers. But the model should hold.

Killer Defect Economics is also an important area where the value of addressing them is misunderstood. It comes in part from the belief that all

process steps should add value to the wafer or be eliminated. At face value this cannot be true because, how do you explain the existence of process diagnostics, as it adds no value to the wafer. If you find a killer defect, the die is still dead. Finding the defect can add no value to the die or wafer you are inspecting because it is lost — it's spilt milk. But this is exactly where the value-added hypothesis of manufacturing economics goes wrong: because it is statics, not dynamics.

You can understand this clearly with the statement, '*if you believe process diagnostics adds no value, stop inspecting, and comeback in a month to tell me how your business is*.' Every time I have said this, the response is, '*but we'll have no yields*.' The answer tells you immediately that *value assurance* is just as important as being *value additive*.

Value assurance is important at the first order because it prevents you from adding value to product that has and will never have value. In plain words, it keeps you from feeding dead horses. Worse, since it's a semiconductor process, by the time it gets to test it's as if you've been feeding the dead horse for 8-12 weeks.

It is in dynamics that you find where process diagnostics begins to add value. To add value, the knowledge from finding a defect must be actionable. For example, you find a killer defect and classify it as a litho hot spot. The next step is in identifying if the root cause is due to the reticle, optics of the scanner, the resist processing, or etching. Once you find the root cause, you can eliminate it. That adds value through a yield gain.

Yield gains have huge value because they not only add value, they have a multiplier effect on profits. If we take a typical 300mm wafer at the leading edge, it needs to generate around $3,889 per wafer to generate reasonable profits if it is memory and $8,101 if it is logic. So every 1% of additional yield will generate $39 and $81, respectively, per wafer in additional revenue.

Profit is where the economics of killer defects gets real interesting. Revenue per Wafer is equal to price times the number of finished good devices, so the cost of manufacturing the good die must be burdened with the total cost of making the wafer. Since almost all wafers make it to test, the full cost of manufacturing bad product is sunk. Thus,

$$C_{Gd} = C_W / (N_d * Y) \quad \text{. . . Therefore . . . } C_{Bd} = 0$$

Where:

C_{Gd} = Cost of manufacturing a good die

C_{Bd} = Cost of manufacturing a bad die

C_W = Cost of manufacturing a wafer

N_d = Number of die on the wafer

Y = Die yield

Thus, every bad die that can be converted to a good die via improved yield is virtually pure profit (there is still assembly and test yield, which has a minimal effect). The multiplier effect of yield gains on profit in percent is as follows:

$$\%\Delta Profit = P_{t-1} / \%\Delta Y$$

Where:
P_{t-1} = Profit rate in the period before the yield gain

So, if profits are 10% of revenues and you increase yield by 1%, profits increase by 10%. Assuming a constant PE ratio, the increase in shareholder value is also 10%. At the limit, as profits approach zero, the percentage gain from an increase in yield becomes infinite. These factors are why chip makers are so willing to spend so much in incremental yield improvement.